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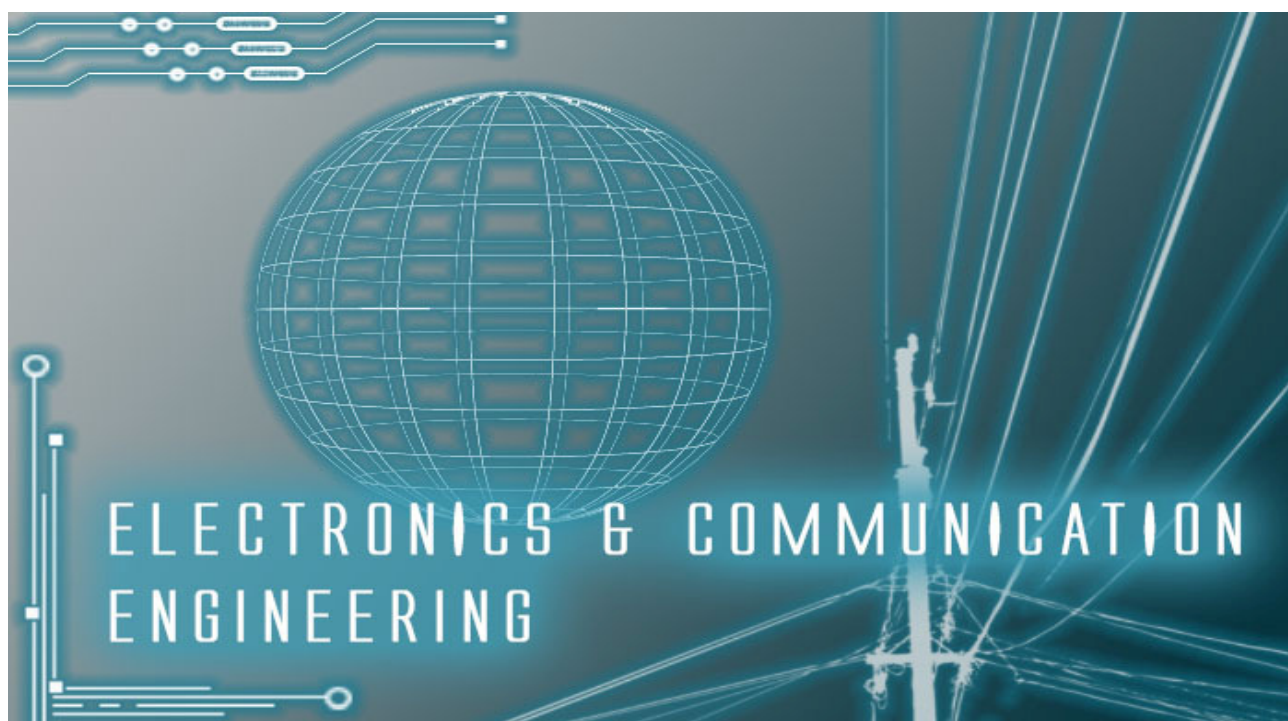
LAB MANUAL

Regulation : 2013

Branch : B.E. – ECE

Year & Semester : II Year / III Semester

EC6311 – ANALOG AND DIGITAL CIRCUITS LABORATORY



ANNA UNIVERSITY CHENNAI

EC6311- Analog and Digital Circuits Laboratory

Regulation 2013

Syllabus

L T P C
0 0 3 2

LIST OF ANALOG EXPERIMENTS:

1. Half Wave and Full Wave Rectifiers, Filters, Power supplies
2. Frequency Response of CE, CB, CC and CS amplifiers
3. Darlington Amplifier
4. Differential Amplifiers- Transfer characteristic, CMRR Measurement
5. Cascode / Cascade amplifier
6. Class A and Class B Power Amplifiers
7. Determination of bandwidth of single stage and multistage amplifiers
8. Spice Simulation of Common Emitter and Common Source amplifiers

LIST OF DIGITAL EXPERIMENTS

9. Design and implementation of code converters using logic gates
 - (i) BCD to excess-3 code and vice versa
 - (ii) Binary to gray and vice-versa
10. Design and implementation of 4 bit binary Adder/ Subtractor and BCD adder using IC 7483
11. Design and implementation of Multiplexer and De-multiplexer using logic gates.
12. Design and implementation of encoder and decoder using logic gates
13. Construction and verification of 4 bit ripple counter and Mod-10 / Mod-12 Ripple counters
14. Design and implementation of 3-bit synchronous up/down counter
15. Implementation of SISO, SIPO, PISO and PIPO shift registers using Flip- flops.

TOTAL PERIODS: 45 PERIODS

INDEX

EXP No	DATE	LIST OF EXPERIMENTS	SIGNATURE	REMARKS
		ANALOG CIRCUITS		
1(a)		HALF WAVE RECTIFIER		
1(b)		FULL WAVE RECTIFIER		
2(a)		FREQUENCY RESPONSE OF COMMON EMITTER AMPLIFIER		
2(b)		FREQUENCY RESPONSE OF COMMON COLLECTOR AMPLIFIER		
2(c)		FREQUENCY RESPONSE OF COMMON BASE AMPLIFIER		
2(d)		FREQUENCY RESPONSE OF COMMON SOURCE AMPLIFIER		
3		DARLINGTON AMPLIFIER		
4		DIFFERENTIAL AMPLIFIER		
5(a)		CASCODE AMPLIFIER		
5(b)		CASCADE AMPLIFIER		
6		SINGLESTAGE AND MULTISTAGE AMPLIFIER (RC COUPLED AMPLIFIER)		
7(a)		CLASS B AMPLIFIER		
7(b)		CLASS A AMPLIFIER		
8		SIMULATION OF CE AND CS AMPLIFIER USING PSPICE		

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EXP No	DATE	LIST OF EXPERIMENTS	SIGNATURE	REMARKS
		DIGITAL CIRCUITS		
1		STUDY OF LOGIC GATES		
2(a)		DESIGN OF ADDER AND SUBTRACTOR		
2(b)		DESIGN AND IMPLEMENTATION OF CODE CONVERTORS		
3		DESIGN OF 4-BIT ADDER AND SUBTRACTOR		
4		DESIGN AND IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER		
5		DESIGN AND IMPLEMENTATION OF ENCODER AND DECODER		
6		CONSTRUCTION AND VERIFICATION OF 4 BIT RIPPLE COUNTER AND MOD 10/MOD 12 RIPPLE COUNTER		
7		DESIGN AND IMPLEMENTATION OF 3 BIT SYNCHRONOUS UP/DOWN COUNTER		
8		DESIGN AND IMPLEMENTATION OF SHIFT REGISTER		

INTRODUCTION ABOUT CIRCUITS AND SIMULATION LAB

CIRCUITS LAB

BREAD BOARD:

In order to build the circuit, a digital design kit that contains a power supply, switches for input, light emitting diodes (LEDs), and a breadboard will be used. Make sure to follow your instructor's safety instructions when assembling, debugging, and observing your circuit. You may also need other items for your lab such as: logic chips, wire, wire cutters, a transistor, etc. Exhibit 1.2 shows a common breadboard, while Exhibit 1.3 shows how each set of pins are tied together electronically. Exhibit 1.4 shows a fairly complex circuit built on a breadboard. For these labs, the highest voltage used in your designs will be five volts or +5V and the lowest will be 0V or ground.



The breadboard

The breadboard is typically a white piece of plastic with lots of tiny little holes in it. You stick wires and component leads into the holes to make circuits. Some of the holes are already electrically connected with each other. The holes are 0.1 inch apart, which is the standard spacing for leads on integrated circuit dual in-line packages. You will verify the breadboard internal connections in this lab.

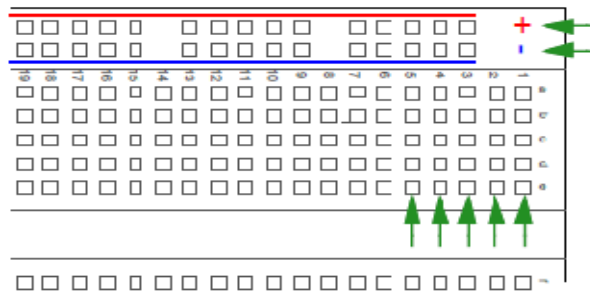
A few words of caution regarding the use of the breadboard:

- Keep the power off when wiring the circuit.
- Make sure to keep things neat, as you can tell from Exhibit 1.4, it is easy for designs to get complex and as a result become difficult to debug.
- Do not strip more insulation off of the wires used than is necessary. This can cause wires that are logically at different levels to accidentally touch each other. This creates a short circuit.
- Do not push the wires too far into each hole in the breadboard as this can cause two different problems.

- The wire can be pushed so far that only the insulation of the wire comes into contact with the breadboard, causing an open circuit.
- Too much wire is pushed into the hole; it curls under and ends up touching another component at a different logical level. This causes a short circuit.
- Use the longer outer rows for +5V on one side and ground on the other side.
- Wire power to the circuit first using a common color (say red) for +5V and another (black) for ground.

Laboratory Procedures, Measurements and Questions

Record your data and the answers to questions on a separate sheet (or sheets) of paper and hand it in at recitation section when the lab is due. You will also have to bring your breadboard with designated circuits on it to your recitation section the week the lab is due.



Procedure 1 Continuity Check (5 points)

Use your multimeter to verify the connections in your breadboard in the first 5 columns and the top two rows of the breadboard as indicated on the diagram below

Set your multimeter on resistance. To find out if any two holes are connected, measure the resistance between them with the multimeter.

- a. **(2 points)** Measure and record the resistance between two holes in a row of 5 connected holes. Measure and record the resistance between two holes at the opposite ends of a long side row (+ or -). Explain the difference (or lack thereof).
- b. **(2 points)** What resistance did you measure between unconnected holes? What did your multimeter read?
- c. **(1 point)** Does it make a difference which probe goes in which hole?

Some hints on measuring resistance:

Never try to measure resistance in energized circuits (ones with the power on). You won't get an accurate value and you could damage your multimeter or the circuit. Your multimeter probes probably

don't fit into the breadboard holes. Stick the stripped end of a wire into each hole, and touch the other stripped ends of the wires with the multimeter probes. If you have clips at the end of your multimeter leads, or you bought those optional alligator clips, you can clip on to the ends of the wires and move the wires from hole to hole. Resistor leads also work for this purpose, but make sure you are not measuring the resistor resistance as well as the breadboard resistance.

Because the multimeter uses a low voltage to measure resistance, you can safely use your fingers to press the wires to the multimeter probes to be sure you have a good contact. If you do, though, you will put your body in parallel with the resistance you are measuring. This can be important for certain large values of resistance, those near or greater than your body resistance. It's usually not a problem for continuity checks.

- Switch the multimeter to off or to the voltage setting when you are not actively measuring resistance. This minimizes battery use in the multimeter and is also a generally safer practice.

CIRCUIT SIMULATION

A common tool (computer aided design or CAD / electronic design automation or EDA software) for the electronic circuit designer is circuit simulation software. Although most often called simply a simulator, it is a software application that typically may include many functions beyond electrical circuit simulation, including schematic capture, printed circuit board layout, and bill of materials generation.

Most circuit simulator software grew out of a public domain program called SPICE (Simulation Program with Integrated Circuit Emphasis) developed at UC Berkeley[1] in the 1970s. The original SPICE program operated in a batch mode and was text based. That is, the user created a text file which described the circuit using a special circuit netlist syntax. This file also included simulation directives which told the software what type of simulation is to be performed. The SPICE program read the input file, performed the appropriate analyses, and produced a text output file that contained the results.

Over time EDA companies began adding graphical “back-ends” that could produce better looking graphs and plots of the simulation results. A next obvious step was to add a graphical interface for building the circuit (GUI). This had the dual benefit of both describing the circuit for the simulation engine (generating the SPICE net list) and allowing for the production of publication quality schematic diagrams. Some of the early popular graphical versions included PSpice and Electronics Workbench (EW being the precursor to Multisim).

More recent features include instrumentation simulation. That is, simulations of real world commercial measurement devices may be used as part of the circuit simulation. In this way, a sort of “virtual lab bench” may be created. Some packages, such as Fritzing[2], also include physical imagery of devices and proto-boards. With this feature, the circuit being designed will look very similar to the actual circuit sitting on your lab bench. That is, if a transistor is used in the simulation, it will look like a real transistor instead of the standard schematic symbol. While this may initially appear to be very useful, especially for beginners, in practical terms it sometimes slows down the design process by making the schematic less clear and more cluttered to the user.

PROCEED AS FOLLOWS TO OBTAIN THE ANSWER USING PSPICE.

1. Run the CAPTURE program.
2. Select File/New/Project from the File menu.
3. On the New Project window select Analog or Mixed A/D, and give a name to your project then click OK.
4. The Create PSpice Project window will pop up, select Create a blank project, and then click OK.
5. Now you will be in the schematic environment where you are to build your circuit.
6. Select Place/Part from the Place menu.
7. Click ANALOG from the box called Libraries:, then look for the part called R. You can do it either by scrolling down on the Part List: box or by typing R on the Part box. Then click OK.
8. Use the mouse to place the resistor where you want and then click to leave the resistor there.
You can continue placing as many resistors as you need and once you have finished placing the resistors right-click your mouse and select end mode.
9. To rotate the components there are two options:
 - Rotate a component once it is placed: Select the component by clicking on it then Ctrl-R
 - Rotate the component before it is placed: Just Ctrl-R.
10. Select Place/Part from the Place menu.
11. Click SOURCE from the box called Libraries:, then look for the part called VDC. You can do it either by scrolling down on the Part List: box or by typing VDC on the Part box, and then click OK. Place the Source.
12. Repeat steps 10 - 12 to get and place a current source named IDC.
13. Select Place/Wire and start wiring the circuit. To start a wire click on the component terminal

where you want it to begin, and then click on the component terminal where you want it to finish. You can continue placing wires until all components are wired. Then right-click and select end wire.

14. Select Place/Ground from the Place menu, click on GND/CAPSYM. Now you will see the ground symbol. Type 0 on the Name: box and then click OK. Then place the ground. Wire it if necessary.
16. Now change the component values to the required ones. To do this you just need to double-click on the parameter you want to change. A window will pop up where you will be able to set a new value for that parameter.
17. Once you have finished building your circuit, you can move on to the next step – prepare it for simulation.
18. Select PSpice/New Simulation Profile and type a name, this can be the same name as your project, and click Create.
19. The Simulations Settings window will now appear. You can set up the type of analysis you want PSpice to perform. In this case it will be Bias Point. Click Apply then OK.
20. Now you are ready to simulate the circuit. Select Pspice /Run and wait until the Pspice finishes. Go back to Capture and see the voltages and currents on all the nodes.
21. If you are not seeing any readout of the voltages and currents then select PSpice/Bias Point/Enable Bias Voltage Display and PSpice/Bias Point/Enable Bias Current Display. Make sure that PSpice/ Bias Point/Enable is checked.

INTRODUCTION ABOUT DIGITAL LABORATORY

In today's modern world, the usage of digital technology is mandatory and unavoidable, applications such as internet, wireless broadcasting systems, Smart Television, computers, industry automation systems, music players etc., are really very reliable and accurate in quality and performance.

In this Lab, we learn the fundamental aspects of digital mathematical and logical operations by hardware and software (HDL simulator) methodologies.

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output. OR, AND and NOT are basic gates. NAND and NOR are known as universal gates.

A half adder has two inputs for the two bits to be added and two outputs one from the sum 'S' and other from the carry 'c' into the higher adder position. Above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND gate.

A conversion circuit must be inserted between the two systems if each uses different codes for same information. Thus, code converter is a circuit that makes the two systems compatible even though each uses different binary code.

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of next full adder in chain.

The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determine their relative magnitude.

A parity bit is used for detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number is either even or odd. The message including the parity bit is transmitted and then checked at the receiver ends for errors.

An error is detected if the checked parity bit doesn't correspond to the one transmitted. The circuit that generates the parity bit in the transmitter is called a 'parity generator' and the circuit that checks the parity in the receiver is called a 'parity checker'.

Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

An encoder is a digital circuit that perform inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generates the binary code corresponding to the input value.

A decoder is a multiple input multiple output logic circuits which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code.

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between a register and a counter. There are two types of counter, synchronous and asynchronous. A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop.

ANALOG EXPERIMENTS

EX.NO:1(a)**DATE:****HALF WAVE RECTIFIER****AIM:**

To rectify the AC signal in half wave rectifier with and without capacitor filter.

APPARATUS REQUIRED :

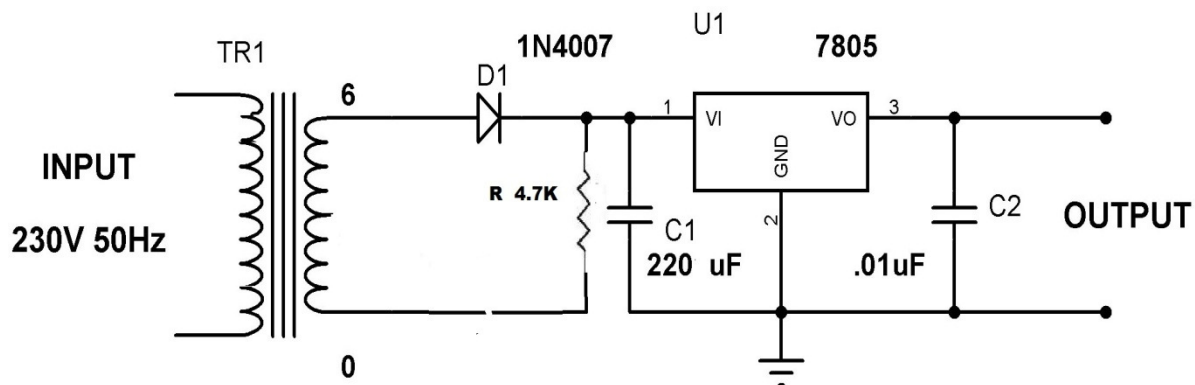
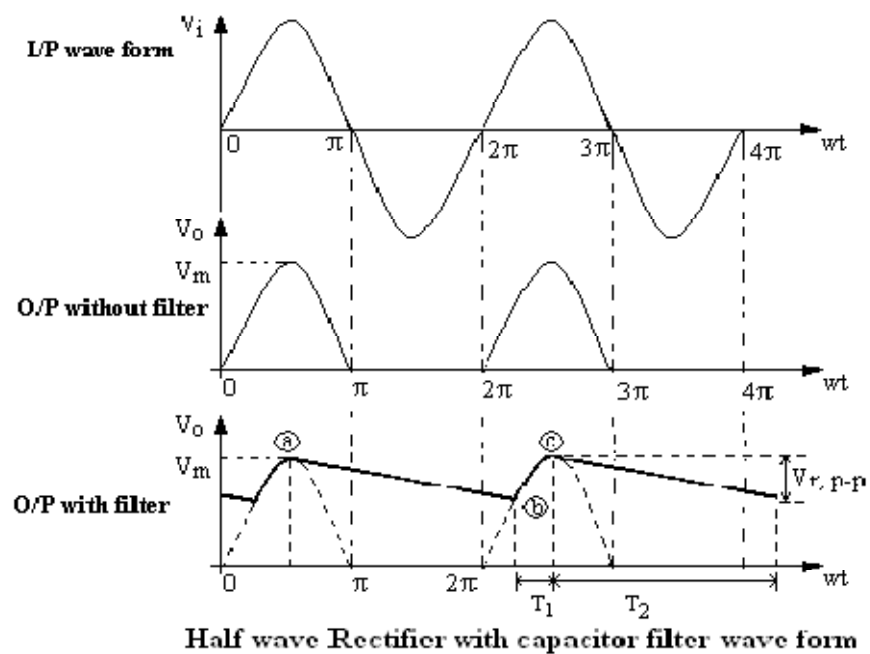
S.No	APPARATUS	RANGE	QUANTITY
1	Transformer	6-0-6 v	1
2	CRO	(0-30)MHz	1
3	Resistors	4.7 k	Each 1
4	Diode	IN4007	1
5	IC	7805(positive)	1
6	Capacitors	220 μ F,0.01 μ F	Each 1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

PROCEDURE:**Without Filter:**

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz.
3. Note down the peak value V_M of the signal observed on the CRO.
4. Switch the CRO into DC mode and observe the waveform.
5. Connect load resistance at 1K Ω and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.

With Filter:

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure.

HALF WAVE RECTIFIER CIRCUIT DIAGRAM:**MODEL GRAPH:**

TABULATION:

Signals	Amplitude (volt)	Time period (sec)
Input signal		
Output signal		
Without filter		
With filter		

RESULT:

Thus the AC signal is rectified in half wave rectifier with and without capacitor filter and the input and output signals are plotted in graph.

EX.NO:1(b)**DATE:****FULL WAVE RECTIFIER****AIM:**

To rectify the AC signal in full wave rectifier with and without capacitor filter.

APPARATUS REQUIRED :

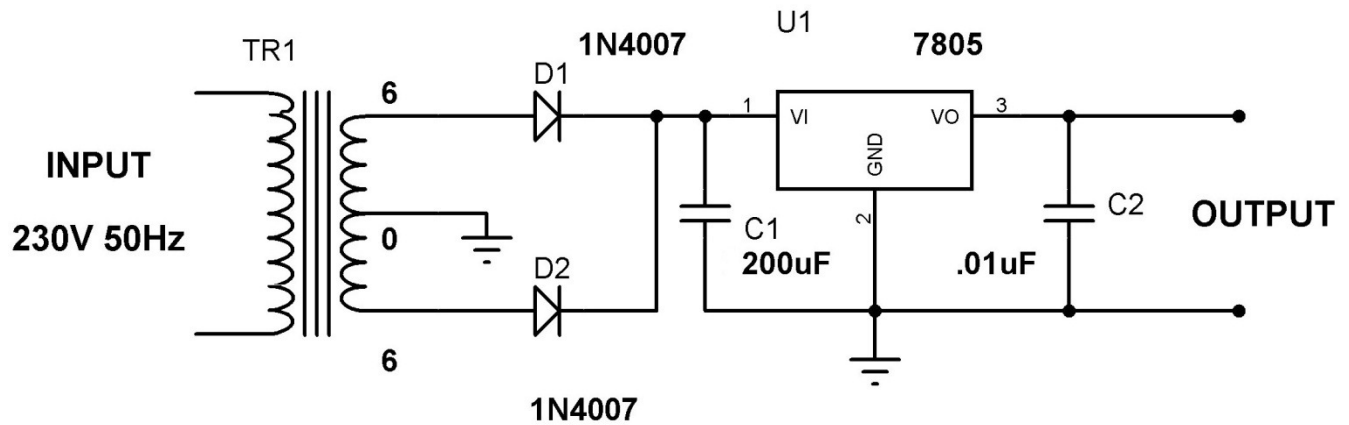
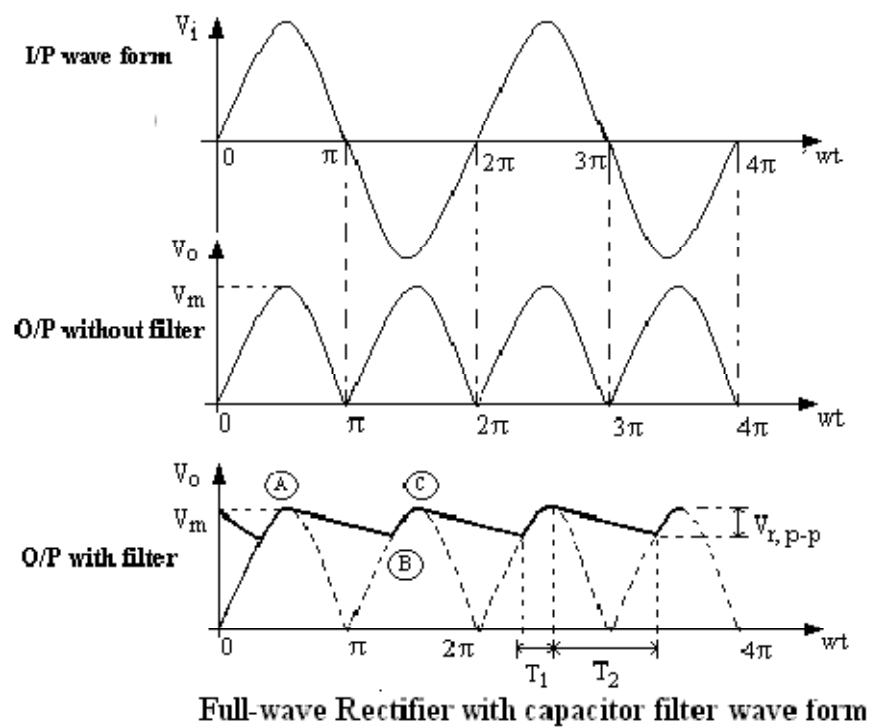
S.No	APPARATUS	RANGE	QUANTITY
1	Transformer	6-0-6 v	1
2	CRO	(0-30)MHz	1
3	Diode	IN4007	2
4	IC	7805(positive)	1
5	Capacitors	220 μ F,0.01 μ F	Each 1
6	Bread Board	-	1
7	Connecting Wires	Single strand	as required

PROCEDURE:**Without filter:**

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz.
3. Note down the peak value V_M of the signal observed on the CRO.
4. Switch the CRO into DC mode and observe the waveform.
5. Connect load resistance at 1K Ω and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.

With filter:

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure.

FULL WAVE RECTIFIER CIRCUIT DIAGRAM:**MODEL GRAPH:**

TABULATION:

Signals	Amplitude (volt)	Time period (sec)
Input signal		
Output signal		
Without filter		
With filter		

RESULT:

Thus the AC signal is rectified in full wave rectifier with and without capacitor filter and the input and output signals are plotted in graph.

EX.NO:2(a)**DATE:****FREQUENCY RESPONSE OF COMMON EMITTER AMPLIFIER****AIM:**

To design a Common Emitter amplifier with self bias and determine the voltage gain to plot the frequency response.

- a. Gain of the amplifier
- b. Bandwidth of the amplifier
- c. Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	60k Ω , 1k Ω , 2.2k Ω , 10k Ω	Each 1
4	Power supply	(0-30)V	1
5	Transistors	BC 107	1
6	Capacitors	10 μ F	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A common emitter amplifier is type of BJT amplifier which increases the voltage level of the applied input signal V_{in} at output of collector. The CE amplifier typically has a relatively high input resistance (1 - 10 K Ω) and a fairly high output resistance. Therefore it is generally used to drive medium to high resistance loads. It is typically used in applications where a small voltage signal needs to be amplified to a large voltage signal like radio receivers.

The input signal V_{in} is applied to base emitter junction of the transistor and amplifier output V_o is taken across collector terminal. Transistor is maintained at the active region by using the resistors R_1, R_2 and R_c . A very small change in base current produces a much larger change in collector current.

The output V_o of the common emitter amplifier is 180 degrees out of phase with the applied the input signal V_{in} .

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CE amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CE amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH} /2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for at least 20 different values for the considered range.
5. The voltage gain is calculated as

$$A_v = 20\log (V_o/V_i) \text{ dB}$$

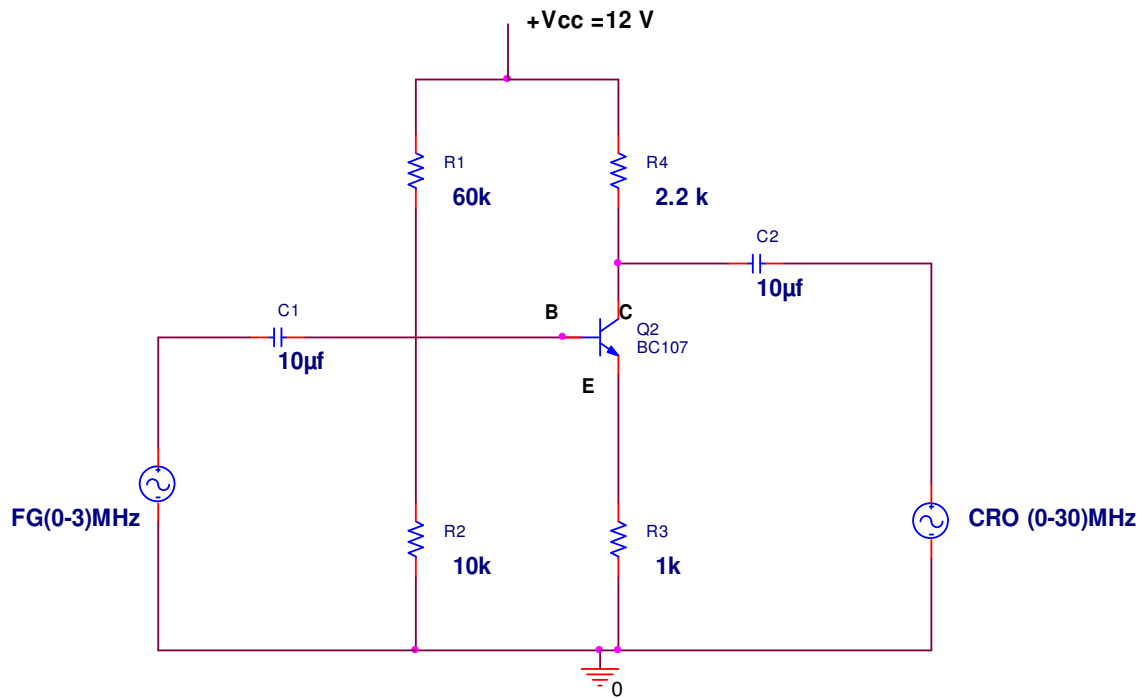
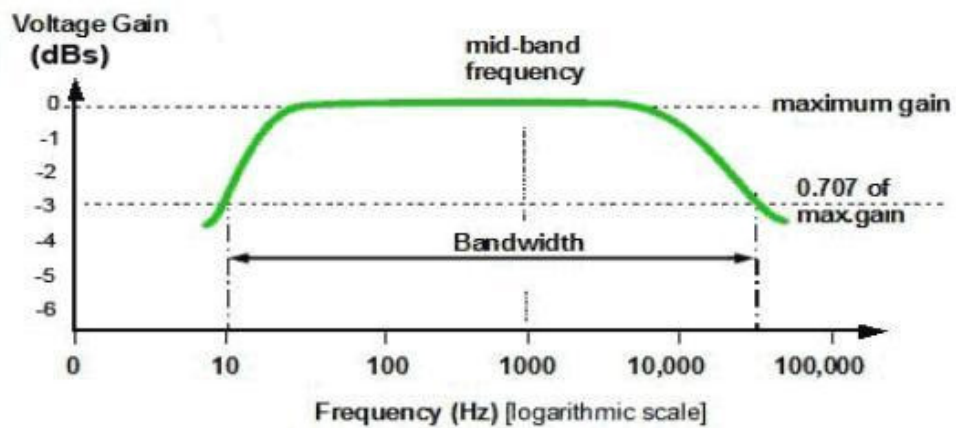
6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.

$$\text{Bandwidth, BW} = f_2 - f_1$$

where

f_1 lower cut-off frequency

f_2 upper cut-off frequency

COMMON EMITTER CIRCUIT DIAGRAM:**MODEL GRAPH :**

FREQUENCY (in Hz)	OUTPUT $V_o(V)$	Gain in dB= $20\log(V_o/V_{in})$ dB
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TABULATION:

Input voltage constant (v_{in}) =

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RESULT:

Thus the Common Emitter amplifier was constructed and the frequency response curve has been plotted.

EX.NO:2(b)

DATE:

FREQUENCY RESPONSE OF COMMON COLLECTOR AMPLIFIER

AIM:

To design a Common Collector amplifier with self bias and determine the voltage gain to plot the frequency response.

- a. Gain of the amplifier
- b. Bandwidth of the amplifier
- c. Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	60k Ω , 1k Ω , 2.2k Ω , 10k Ω	Each 1
4	Power supply	(0-30)V	1
5	Transistors	BC 107	1
6	Capacitors	10 μ F	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A common collector amplifier is type of BJT amplifier which increases the voltage level of the applied input signal V_{in} at output of collector.

The CC amplifier typically has a relatively high input resistance (1 - 10 K Ω) and a fairly high output resistance. Therefore it is generally used to drive medium to high resistance loads. It is typically used in applications where a small voltage signal needs to be amplified to a large voltage signal like radio receivers.

The input signal V_{in} is applied to base emitter junction of the transistor and amplifier output V_o is taken across collector terminal. Transistor is maintained at the active region by using the resistors R_1, R_2 and R_c . A very small change in base current produces a much larger change in collector current.

The output V_o of the common emitter amplifier is 180 degrees out of phase with the applied the input signal V_{in}

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CC amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CC amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for at least 20 different values for the considered range.
5. The voltage gain is calculated as

$$A_v = 20\log (V_o/V_i) \text{ dB}$$

6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

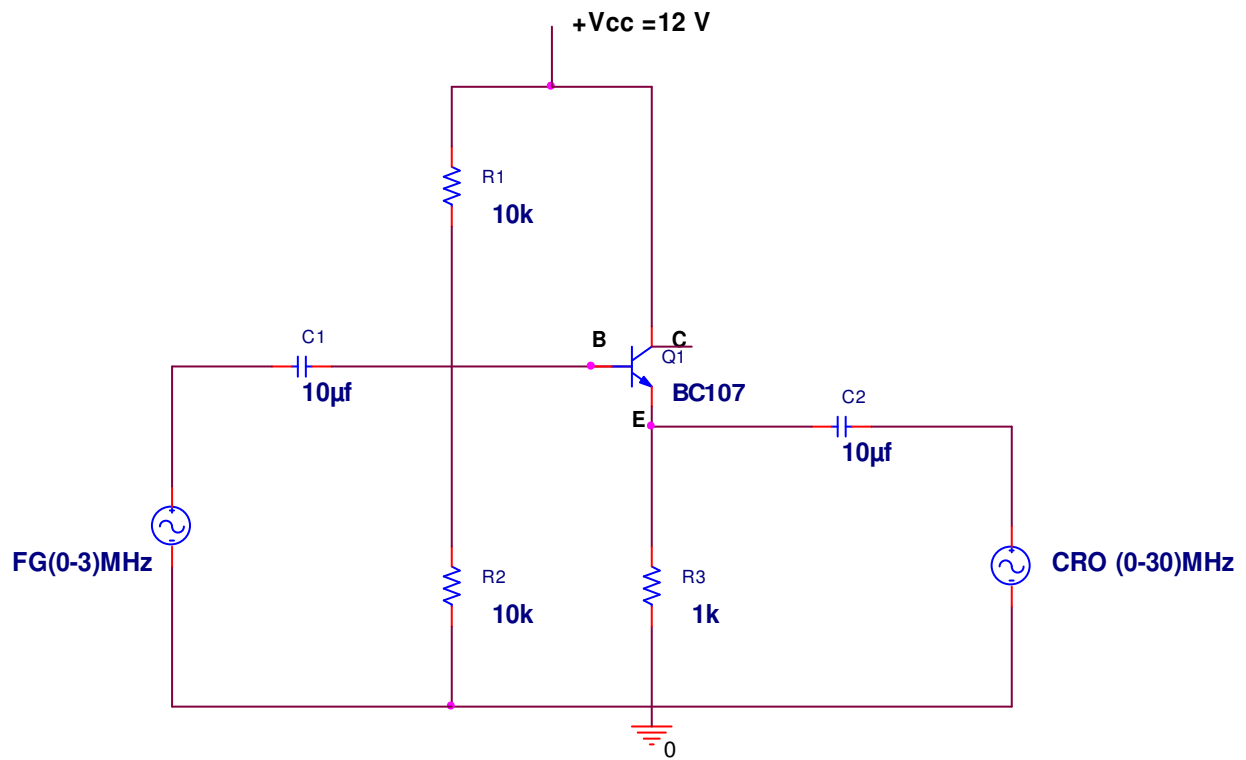
$$\text{Bandwidth, BW} = f_2 - f_1$$

where

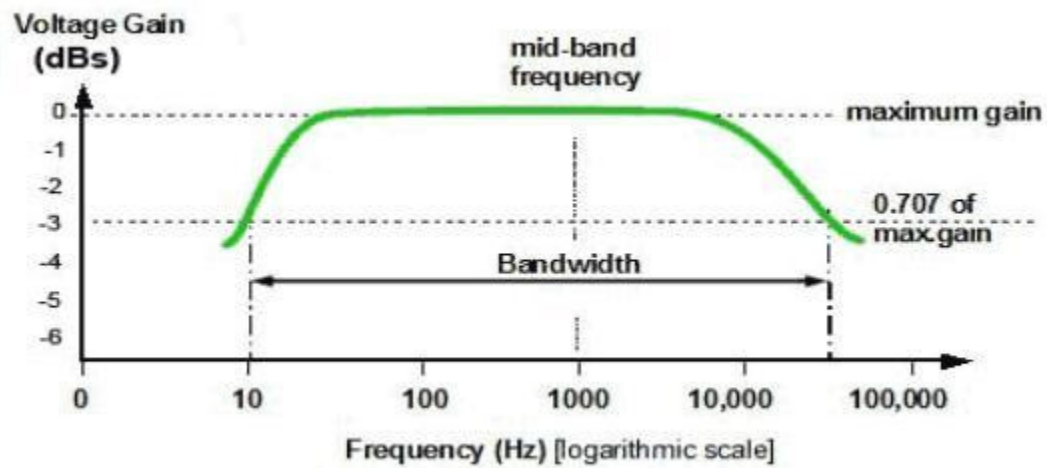
f_1 lower cut-off frequency

f_2 upper cut-off frequency

COMMON COLLECTOR CIRCUIT DIAGRAM:



MODEL GRAPH



TABULATION:

Input voltage constant (v_{in}) =

FREQUENCY (in Hz)	OUTPUT $V_o(V)$	Gain in dB= $20\log(V_o/V_{in})$ dB

RESULT:

Thus the Common Collector amplifier was constructed and the frequency response curve I has been plotted.

EX.NO:2(c)

DATE:**FREQUENCY RESPONSE OF COMMON BASE AMPLIFIER****AIM:**

To design a Common Base amplifier with self bias and determine the voltage gain to plot the frequency response.

- a. Gain of the amplifier
- b. Bandwidth of the amplifier
- c. Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1k Ω , 10k Ω	Each 1
4	Power supply	(0-30)V	1
5	Transistors	BC 107	1
6	Capacitors	10 μ F, 1 μ F	Each 1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A common base amplifier is type of BJT amplifier which increases the voltage level of the applied input signal V_{in} at output of collector.

The Common base amplifier typically has good voltage gain and relatively high output impedance. But the Common base amplifier unlike CE amplifier has very low input impedance which makes it unsuitable for most voltage amplifier. It is typically used as an active load for a cascode amplifier and also as a current follower circuit.

Circuit Operation:

A positive-going signal voltage at the input of a CB pushes the transistor emitter in a positive direction while the base voltage remains fixed, hence V_{be} reduces. The reduction in V_{BE} results in reduction in V_{RC} , consequently V_{CE} increases. The rise in collector voltage effectively rises the output voltage. The positive going pulse at the input produces a positive-going output, hence there is no phase shift from input to output in CB circuit. In the same way the negative-going input produces a negative-going output.

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CB amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CB amplifier using AC analysis.
4. Set the input voltage $V_{in} = V_{MSH} / 2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

$$A_v = 20 \log (V_o/V_i) \text{ dB}$$

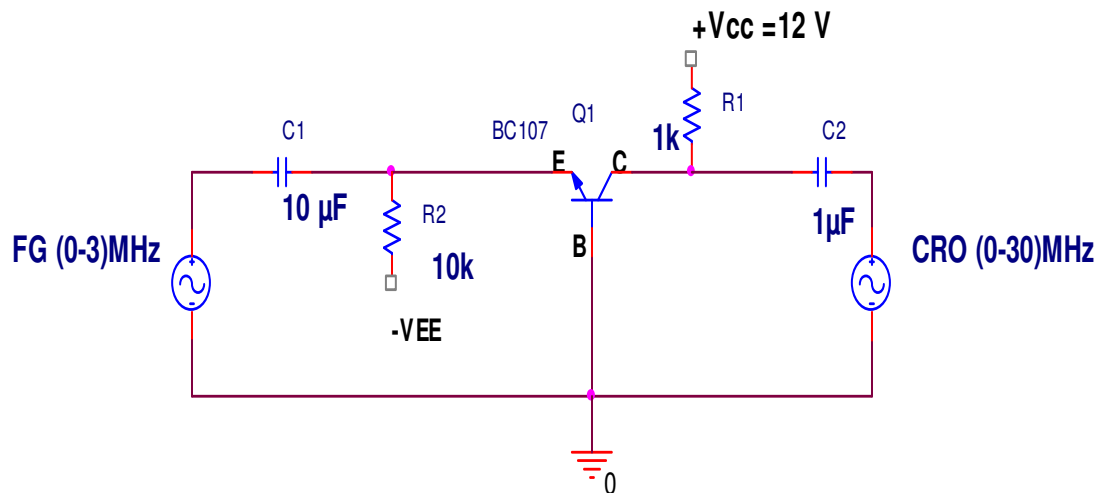
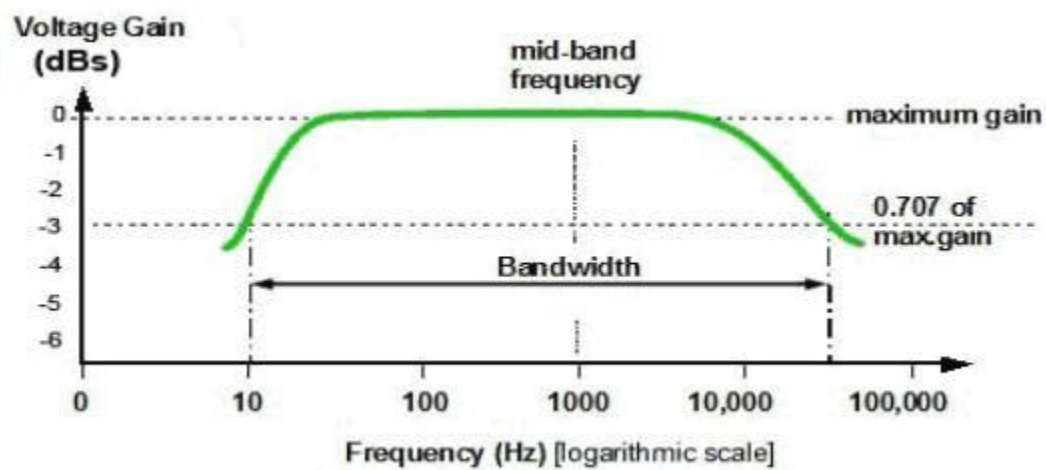
6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

$$\text{Bandwidth, BW} = f_2 - f_1$$

where

f_1 lower cut-off frequency

f_2 upper cut-off frequency

COMMON BASE CIRCUIT DIAGRAM:**MODEL GRAPH :**

TABULATION:**Input voltage constant (V_{in}) =**

FREQUENCY (in Hz)	OUTPUT $V_o(V)$	Gain in dB= $20\log(V_o/V_{in})$ dB

RESULT:

Thus the Common Base amplifier was constructed and the frequency response curve has been plotted.

EX.NO:2(d)**DATE:****FREQUENCY RESPONSE OF COMMON SOURCE AMPLIFIER****AIM:**

To design a Common Source amplifier with self bias and determine the voltage gain to plot the frequency response.

- Gain of the amplifier
- Bandwidth of the amplifier
- Gain -Bandwidth Product

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1k Ω , 10k Ω , 2K Ω ,	Each 1
4	Power supply	(0-30)V	1
5	JFET	BFW10	1
6	Capacitors	10 μ F, 1 μ F	Each 1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

There are three basic types of FET amplifier or FET transistor namely common source amplifier, common gate amplifier and source follower amplifier.

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier.

i) As a transconductance amplifier, the input voltage is seen as modulating the current going to the load.

ii) As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law.

However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CS amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CS amplifier using AC analysis.
4. Set the input voltage $V_{in} = V_{MSH} / 2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

$$A_v = 20 \log (V_o / V_i) \text{ dB}$$

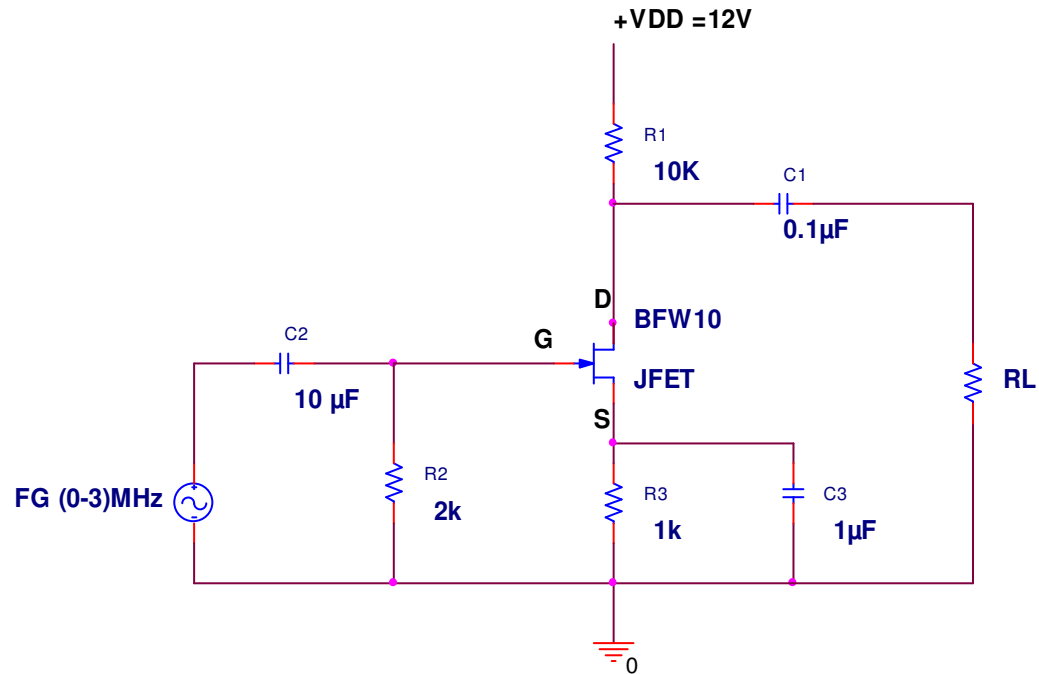
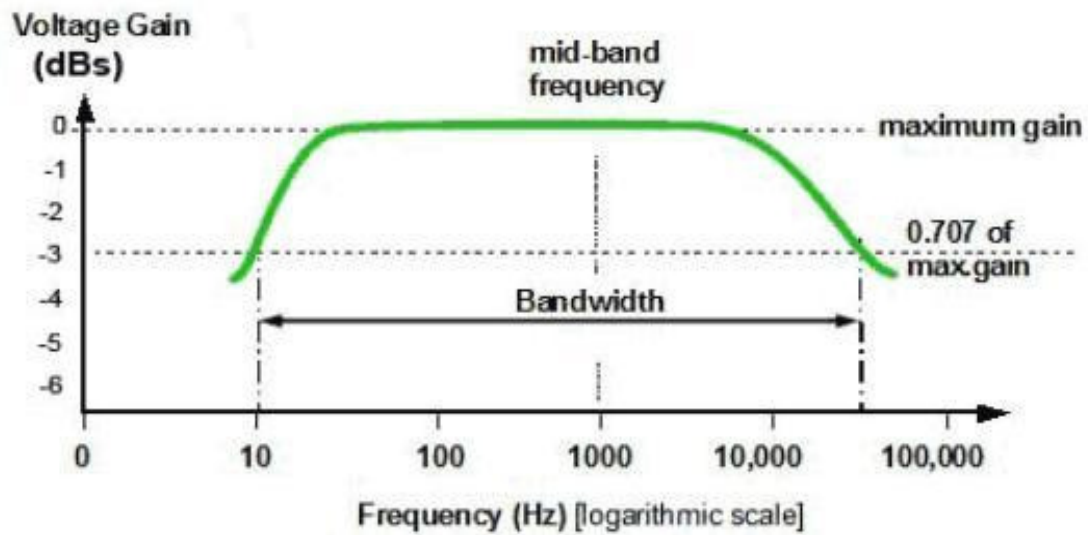
6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

$$\text{Bandwidth, BW} = f_2 - f_1$$

where

f_1 lower cut-off frequency

f_2 upper cut-off frequency

COMMON SOURCE CIRCUIT DIAGRAM:**MODEL GRAPH:**

TABULATION:Input voltage constant (V_{in}) =

FREQUENCY (in Hz)	OUTPUT $V_o(V)$	Gain in dB= $20\log(V_o/V_{in})dB$

RESULT:

Thus the Common Source amplifier was constructed and the frequency response curve I has been plotted.

EX.NO:3**DATE:****DARLINGTON AMPLIFIER****AIM:**

To Design and Construct a BJT amplifier using Darlington pair and to determine its:

- Gain of the amplifier
- Bandwidth of the amplifier
- Gain -Bandwidth Product using frequency response curve

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1k Ω , ,10k Ω ,2K Ω ,	Each 1
4	Power supply	(0-30)V	1
5	JFET	BFW10	1
6	Capacitors	10 μ F,1 μ F	Each 1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

The Darlington transistor (often called a Darlington pair) is compound structure consisting of two bipolar transistors connected in such a way that the First transistor does current amplification of input signal and then it will be fed to the second transistor which performs voltage amplification.

This configuration gives a much higher gain than each transistor taken separately and, in the case of integrated devices, can take less space than two individual transistors because they can use a shared collector. The Darlington amplifier typically has a relatively high input resistance (1 - 10 K Ω) and a fairly high output resistance. Therefore it is generally used to drive medium to high resistance loads. It is typically used in applications where a small voltage signal needs to be amplified to a large voltage signal like radio receivers.

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the Darlington amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to Darlington amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH} / 2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for at least 20 different values for the considered range.
5. The voltage gain is calculated as

$$A_v = 20\log (V_o/V_i) \text{ dB}$$

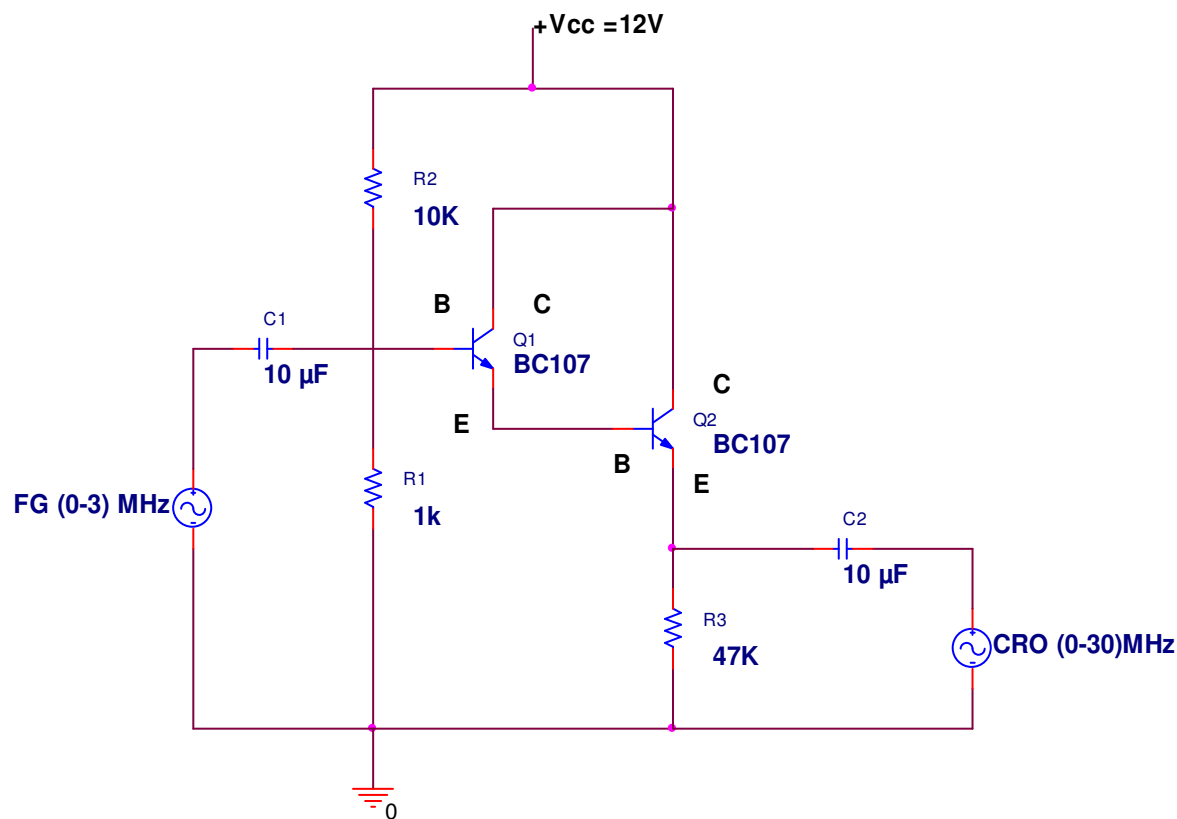
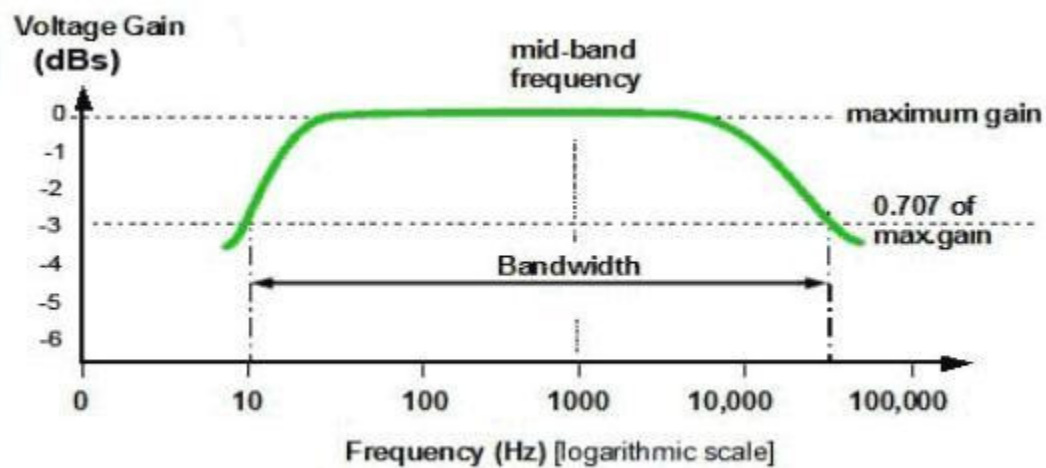
6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

$$\text{Bandwidth, BW} = f_2 - f_1$$

where

f_1 lower cut-off frequency

f_2 upper cut-off frequency

DARLINGTON AMPLIFIER CIRCUIT DIAGRAM:**MODEL GRAPH:**

TABULATION:**Input voltage constant (V_{in}) =**

FREQUENCY (in Hz)	OUTPUT $V_o(V)$	Gain in dB= $20\log(V_o/V_{in})dB$

RESULT:

Thus the Darlington amplifier was constructed and the frequency response curve has been plotted.

EX.NO: 4**DATE:****DIFFERENTIAL AMPLIFIER****AIM:**

To Design and Construct a Differential Amplifier using BJT and to determine its:

- Transfer Characteristics.
- Gain of the amplifier in common mode.
- Gain of the amplifier in differential mode.
- CMRR (Common Mode Rejection Ratio).

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1K Ω , 1K Ω , 10k Ω , 4.7K Ω ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	1
6	Bread Board	-	1
7	Connecting Wires	Single strand	as required

THEORY:

A differential amplifier is a type of electronic amplifier that amplifies the difference between two voltages but does not amplify the particular voltages. The need for differential amplifier arises in many physical measurements where response from D.C to many MHz is required. It is also used in input stage of integrated amplifier.

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the Differential amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to amplifier using AC analysis.
4. Determine the Transfer characteristics of Differential amplifier by plotting the graph for normalized differential input voltage [$(V_{b1} - V_{b2}) / V_T$] vs. Normalized collector current [I_c / I_o].
5. Calculate the voltage gain of differential amplifier for differential mode as

$$A_d = 20 \log (V_o / V_i)$$

Where $V_i = V_1 - V_2$

6. Calculate the voltage gain of differential amplifier for Common mode as

$$A_c = 20 \log (V_o / V_i)$$

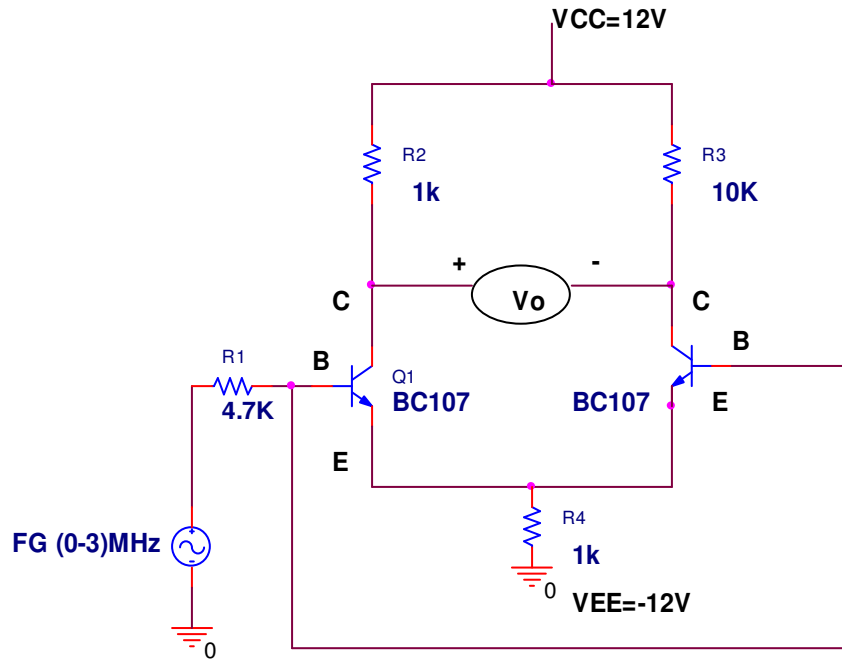
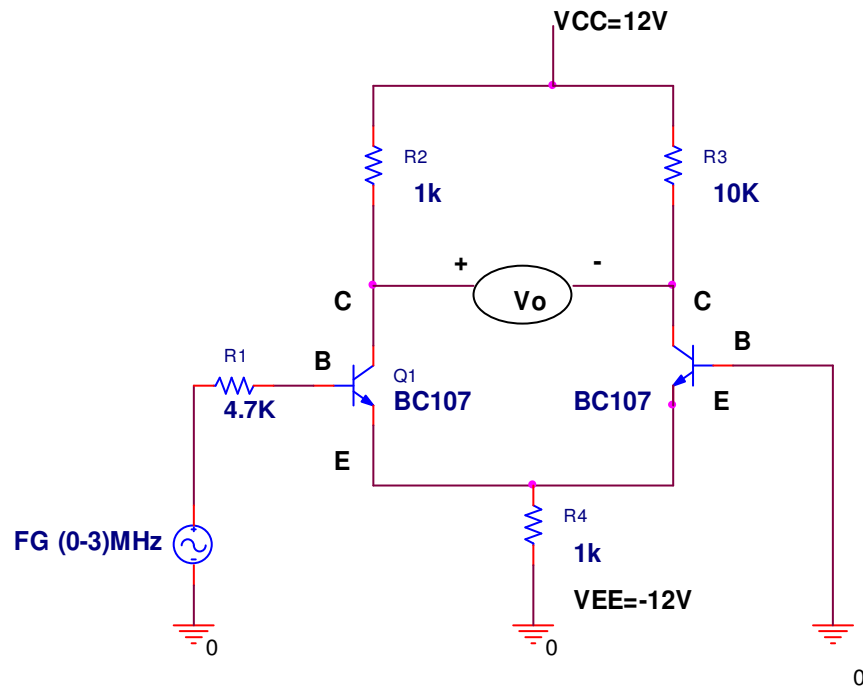
Where $V_i = (V_1 + V_2 / 2)$

7. Find the Common mode rejection ratio of differential amplifier using the formula given below.

$$CMRR = 20 \log_{10} (A_d / A_c)$$

Where A_d - Differential mode gain in dB

A_c – Common Mode gain in dB

COMMON MODE CIRCUIT DIAGRAM:**DIFFERENTIAL MODE CIRCUIT DIAGRAM:**

TRANSFER CHARACTERISTICS CALCULATION:

S.NO	INPUT VOLTAGE $V_I = (V_{B1} - V_{B2})$ IN VOLTS	OUTPUT CURRENT I_{C2} IN AMPERE
1.		
2.		
3.		
4.		
5.		
6.		

RESULT:

Thus the gain of the differential amplifier was constructed and the frequency response curve has been plotted.

EX.NO: 5(a)**DATE:****CASCODE AMPLIFIER****AIM:**

To design and construct a cascode amplifier and to plot the frequency response characteristics.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1K Ω ,	3
		10K Ω ,25K Ω ,270 K Ω ,120 K Ω ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	1
6	Capacitor	0.01 μ f,10mf	2,1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

The cascode configuration has one of two configurations of multistage amplifier. In each case the collector of the leading transistor is connected to the emitter of the following transistor. The arrangement of the two transistors is shown in the circuit diagram. The cascode amplifier consists of CE stage connected in series with CB stage. The arrangement provides a relatively high input impedance with low voltage gain for the first stage to ensure the input miller capacitance is at a minimum, whereas the following CB stage provides an excellent high frequency response.

Features:

1. It provides high voltage gain and has high input impedance.
2. It provides high stability and has high output impedance

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the CE amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to CE amplifier using AC analysis.
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

$$A_v = 20\log (V_o/V_i) \text{ dB}$$

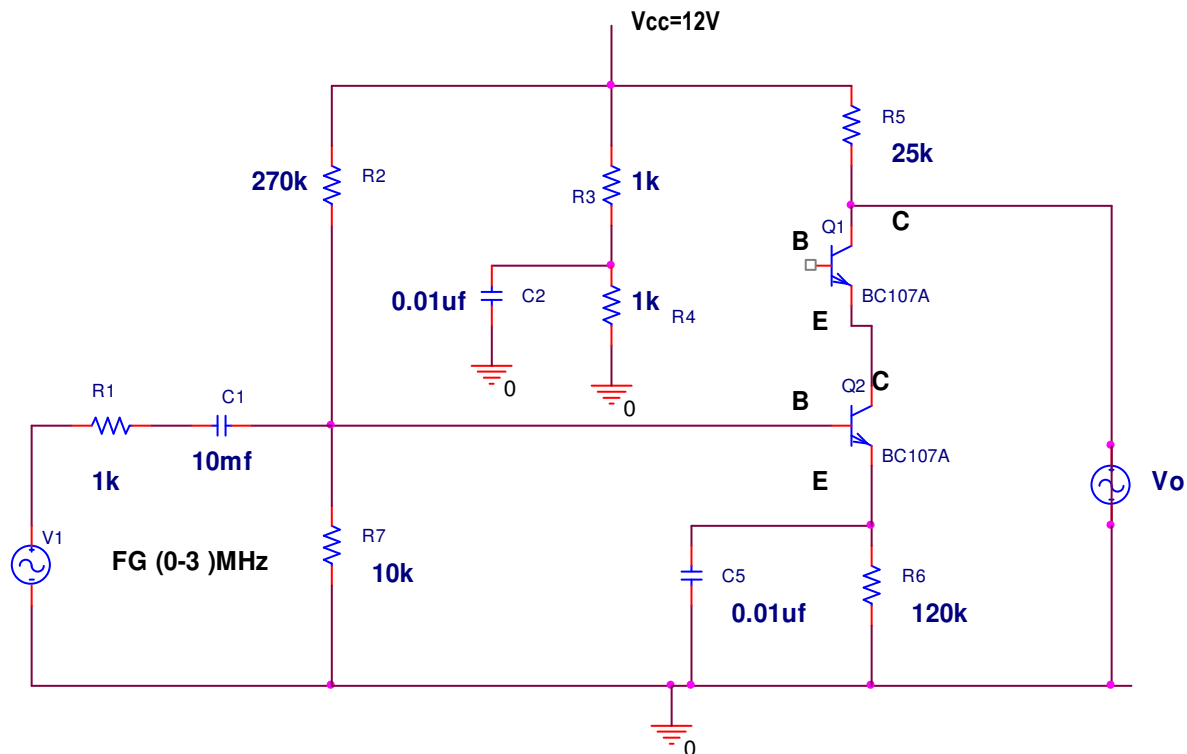
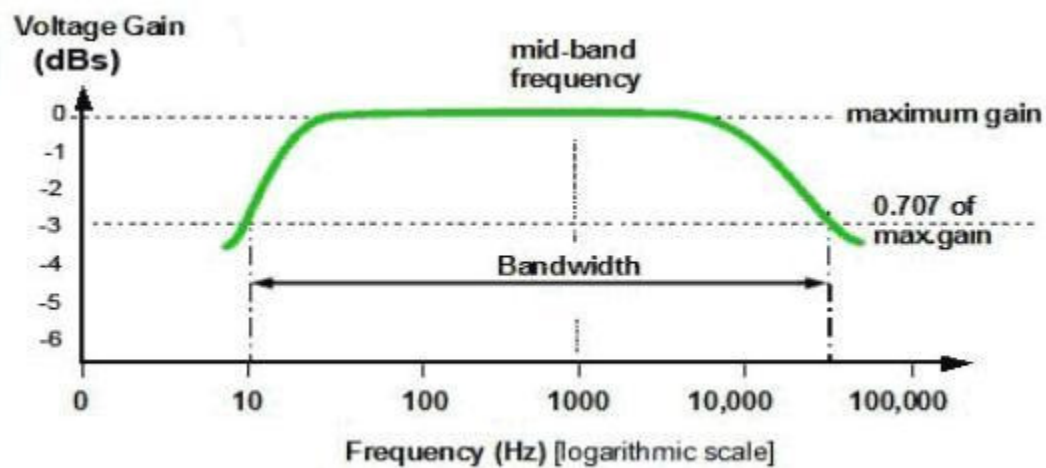
6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

$$\text{Bandwidth, BW} = f_2 - f_1$$

where

f_1 lower cut-off frequency

f_2 upper cut-off frequency

CASCODE AMPLIFIER CIRCUIT DIAGRAM:**MODEL GRAPH :**

TABULATION:

voltage (vin) =	FREQUENCY (in Hz)	OUTPUT V _o (V)	Gain in dB= 20log(V _o /V _{in}) dB	Input constant

RESULT:

Thus the cascode amplifier was constructed and the frequency response curve has been plotted in graph.

EX.NO: 5(b)

DATE:

CASCADE AMPLIFIER

AIM:

To design and construct a cascade amplifier and to plot the frequency response characteristics.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1K Ω ,	3
		10K Ω ,25K Ω ,270 K Ω ,120 K Ω ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	2
6	Capacitor	0.01 μ f,10mf	2,1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A cascade is type of multistage amplifier where two or more single stage amplifiers are connected serially. Many times the primary requirement of the amplifier cannot be achieved with single stage amplifier, because Of the limitation of the transistor parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification. These types of amplifier circuits are employed in designing microphone and loudspeaker

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to amplifier using AC analysis
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

$$A_v = 20\log (V_o/V_i) \text{ dB}$$

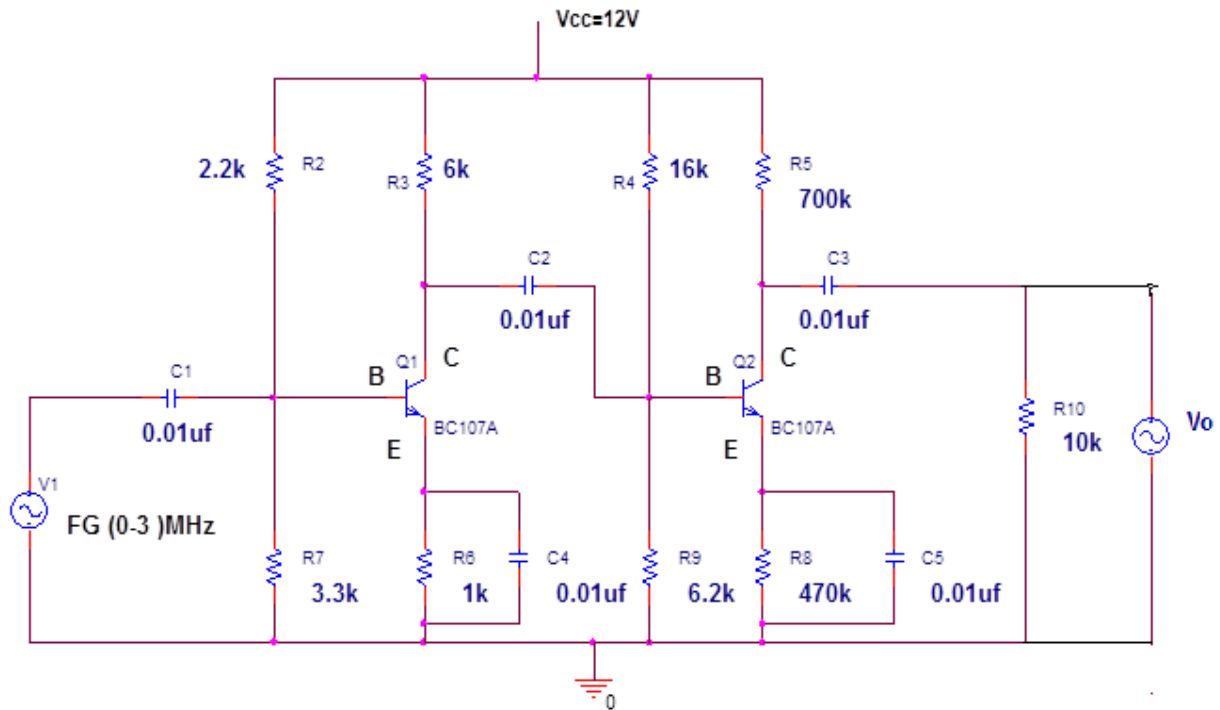
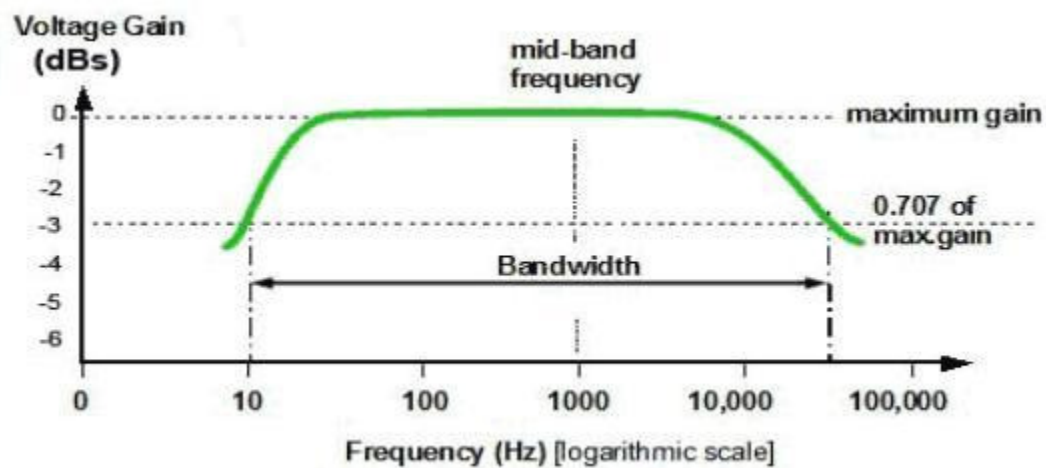
6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

$$\text{Bandwidth, BW} = f_2 - f_1$$

where

f_1 lower cut-off frequency

f_2 upper cut-off frequency

CASCADE AMPLIFIER CIRCUIT DIAGRAM:**MODEL GRAPH :**

TABULATION:

Input voltage constant (v_{in}) =

FREQUENCY (in Hz)	OUTPUT $V_o(V)$	Gain in dB= $20\log(V_o/V_{in})$ dB

RESULT:

Thus the cascade amplifier was constructed and the frequency response curve has been plotted in graph

EX.NO: 6**DATE:**

**SINGLESTAGE AND MULTISTAGE AMPLIFIER
(RC COUPLED AMPLIFIER)**

AIM:

To design and construct a single stage and multistage amplifier and to plot the frequency response characteristics.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1K Ω ,	6
		10K Ω ,25K Ω ,270 K Ω ,120 K Ω ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	2
6	Capacitor	0.01 μ f,10mf,10 μ f	2,1,1
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

It is the most important method of coupling the signal from one to the next stage .The Output signal of the first stage is coupled to the input of next stage through coupling .The coupling network does not affect the quiescent point of the next stage since the coupling capacitor isolate the DC voltage of the first stage from the next stage.

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to amplifier using AC analysis
4. Set the input voltage $V_{in}=V_{MSH}/2$ and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage V_o for atleast 20 different values for the considered range.
5. The voltage gain is calculated as

$$A_v = 20\log (V_o/V_i) \text{ dB}$$

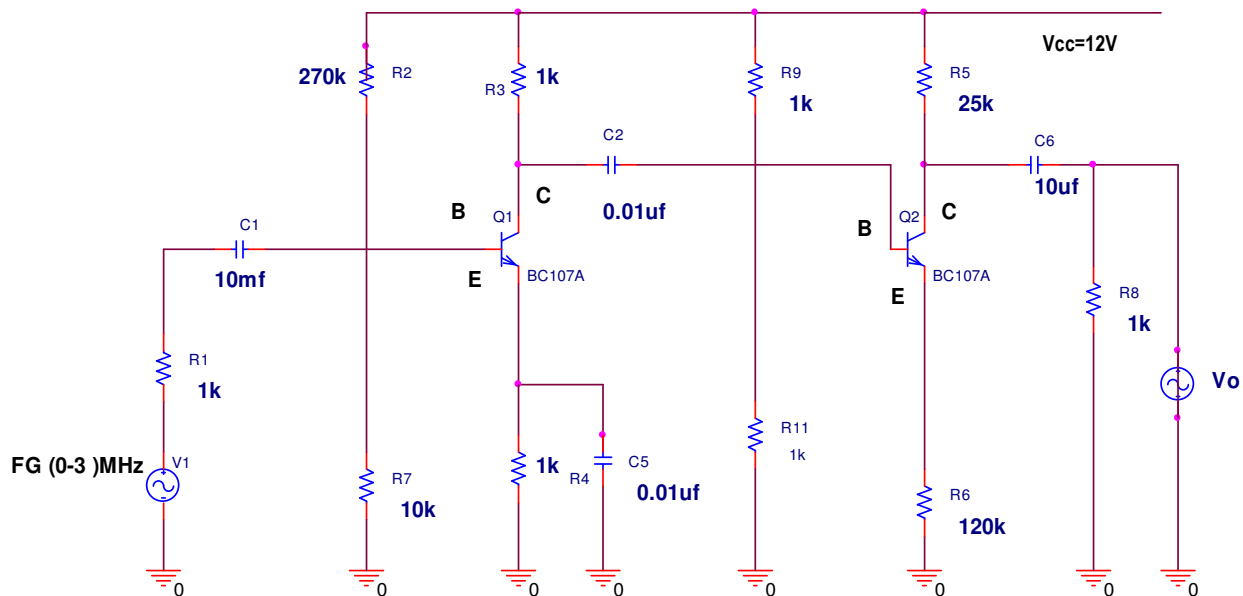
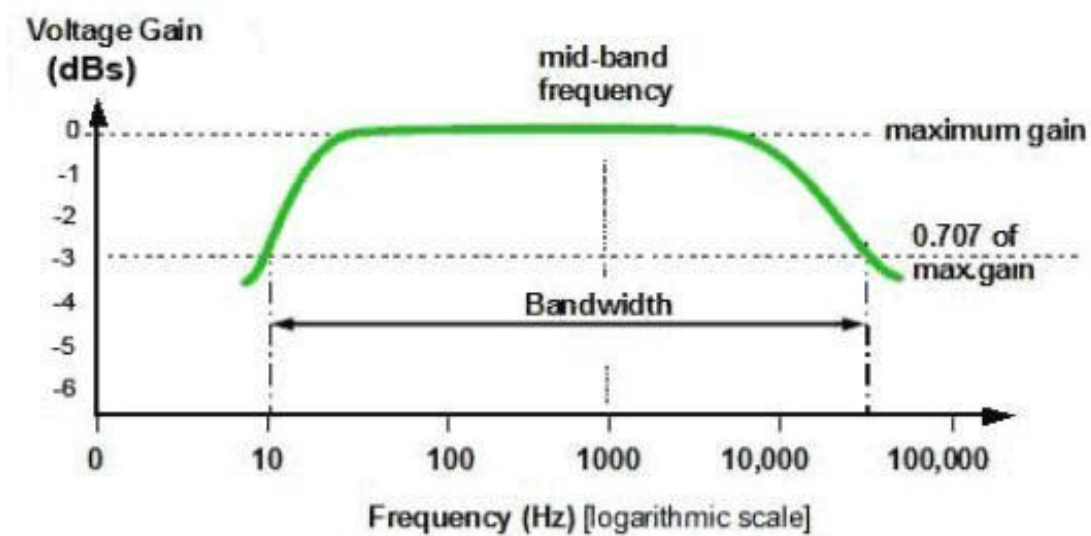
6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

$$\text{Bandwidth, BW} = f_2 - f_1$$

where

f_1 lower cut-off frequency

f_2 upper cut-off frequency

SINGLE STAGE AND MULTISTAGE CIRCUIT DIAGRAM:**MODEL GRAPH :**

TABULATION:**Input voltage constant (v_{in}) =**

FREQUENCY (in Hz)	OUTPUT $V_o(V)$	Gain in dB= $20\log(V_o/V_{in})$ dB

RESULT:

Thus the single stage and multistage amplifier was constructed and the frequency response curve has been plotted in graph.

EX.NO: 7(a)**DATE:****CLASS B AMPLIFIER****AIM:**

To construct a Class B complementary symmetry power amplifier and observe the waveforms with and without cross-over distortion and to compute maximum output power and efficiency.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	4.7K Ω , 1.5K Ω ,	Each 1
4	Power supply	(0-30)V	1
5	Transistor	BC107	2
6	Capacitor	100 μ f,	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

A power amplifier is said to be Class B amplifier if the Q-point and the input signal are selected such that the output signal is obtained only for one half cycle for a full input cycle. The Q-point is selected on the X-axis. Hence, the transistor remains in the active region only for the positive half of the input signal. There are two types of Class B power amplifiers: Push Pull amplifier and complementary symmetry amplifier. In the complementary symmetry amplifier, one n-p-n and another p-n-p transistor is used. The matched pair of transistor are used in the common collector configuration. In the positive half cycle of the input signal, the n-p-n transistor is driven into active region and starts conducting and in negative half cycle, the p-n-p transistor is driven into conduction. However there is a period between the crossing of the half cycles of the input signals, for which none of the transistor is active and output, is zero

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Observe the waveforms and note the amplitude and time period of the input signal and distorted waveforms.
3. Connections are made with proper biasing.
4. Observe the waveforms and note the amplitude and time period of the input signal and output Signal.
5. Draw the waveforms for the readings.
6. Calculate the maximum output power and efficiency.

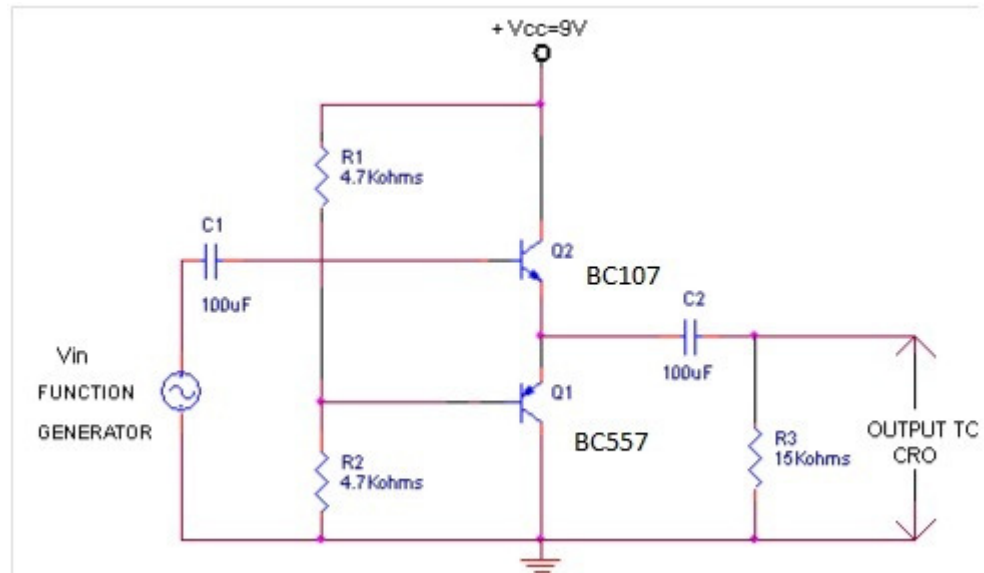
FORMULA:

Input power, $P_{in} = 2V_{cc}I_m/\pi$

Output power, $P_{out} = V_m I_m/2$

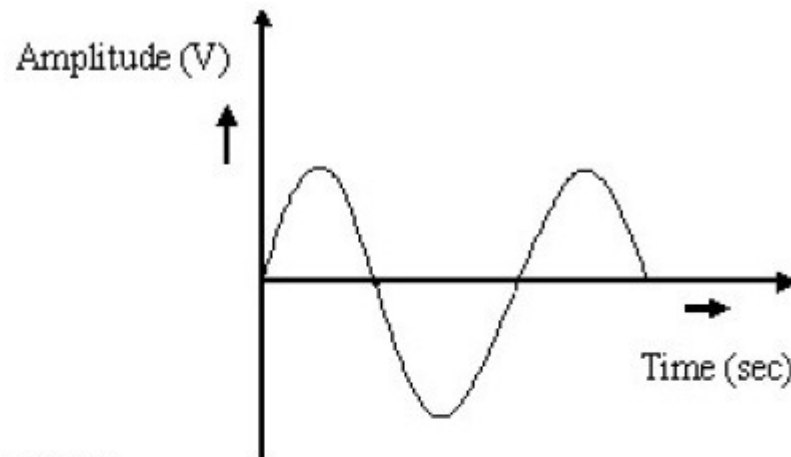
Power Gain or efficiency, $\eta = \pi/4(V_m/V_{cc})^2 \times 100$

CLASS B AMPLIFIER CIRCUIT DIAGRAM:

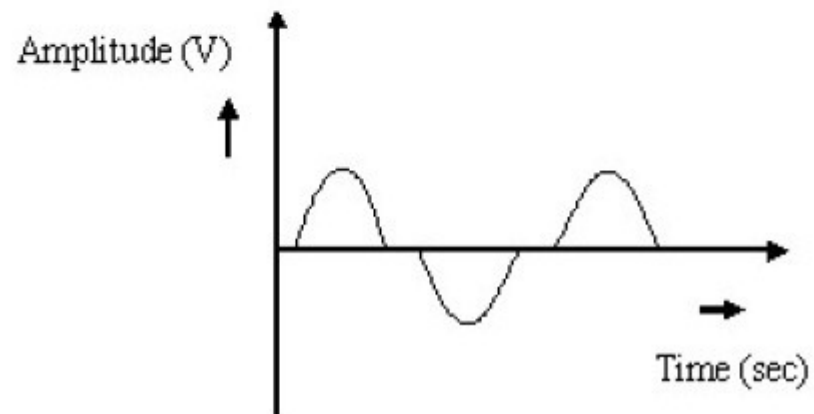


MODEL GRAPH :

INPUT SIGNAL



OUTPUT SIGNAL

**TABULATION:**

Signals	Amplitude (volt)	Time period (sec)
Input signal		
Output signal		

RESULT :

Thus the Class B complementary symmetry power amplifier was constructed and the waveforms values are plotted in graph.

EX.NO: 7(b)

DATE:

CLASS A AMPLIFIER**AIM:**

To construct a Class A power amplifier and observe the waveform and to compute maximum output power and efficiency.

APPARATUS REQUIRED :

S.No	APPARATUS	RANGE	QUANTITY
1	Function Generator	(0-3)MHz	1
2	CRO	(0-30)MHz	1
3	Resistors	1 K Ω ,330 Ω ,220K Ω ,220 Ω	Each 1

4	Power supply	(0-30)V	1
5	Transistor	BC107	1
6	Capacitor	4.7 μ f,	2
7	Bread Board	-	1
8	Connecting Wires	Single strand	as required

THEORY:

The power amplifier is said to be Class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input signal cycle. For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally. The collector current flows for 360 (full cycle) of the input signal. i.e the angle of the collector current flow is 360°.

PROCEDURE:

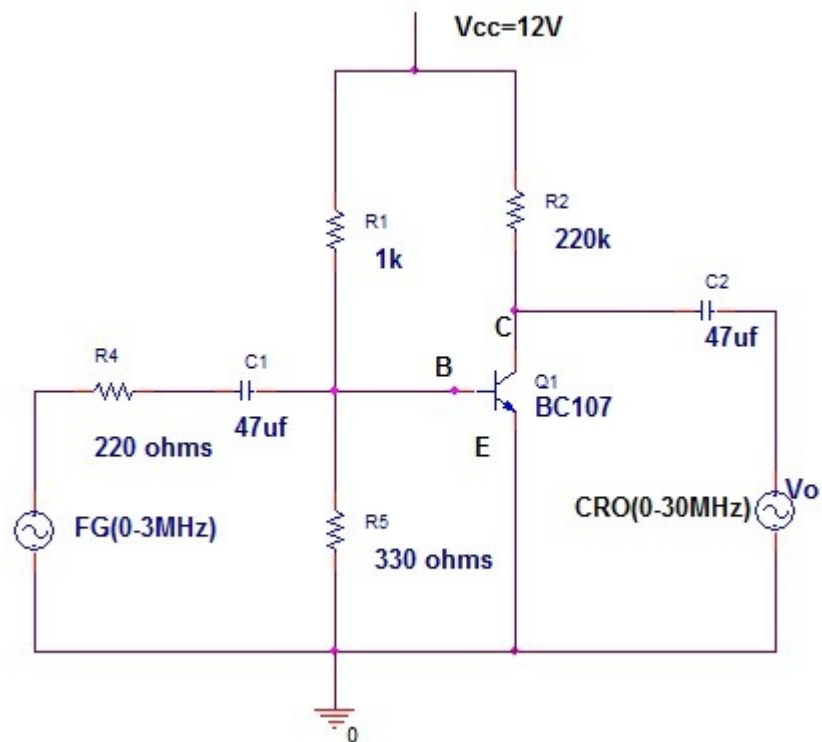
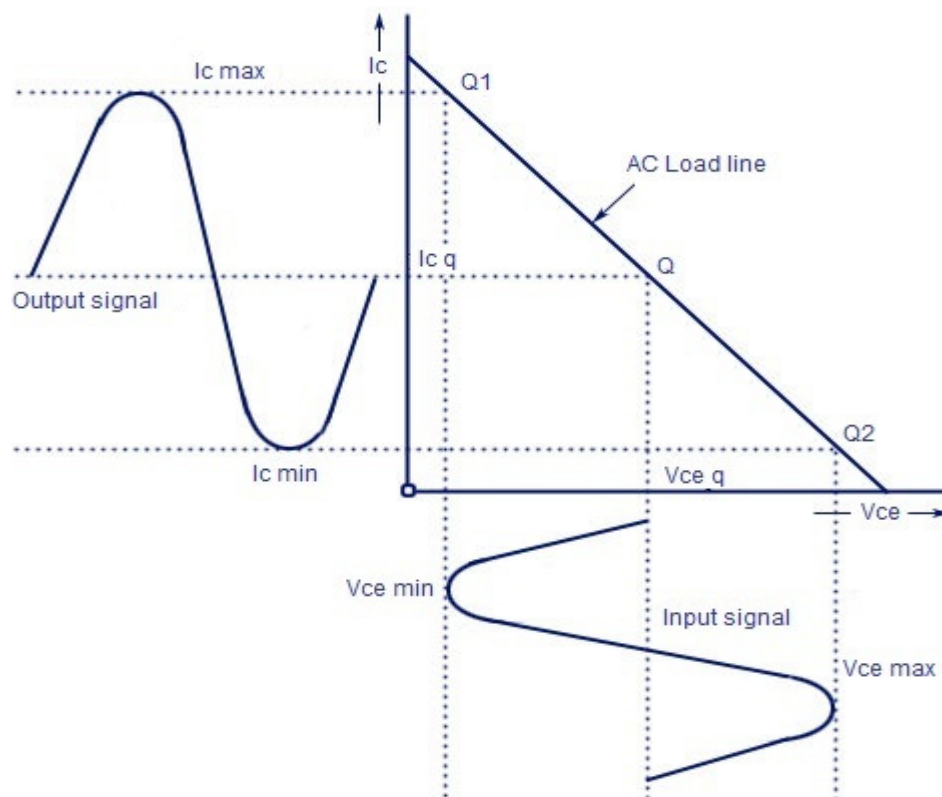
1. Connect the circuit as per the circuit diagram.
2. Set $V_i = 50$ mv, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 10 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) vs Frequency (Hz).

FORMULA

$$\text{Maximum power transfer} = P_{o,\max} = V_o^2 / R_L$$

$$\text{Efficiency } \eta = P_{o,\max} / P_c$$

CLASS A AMPLIFIER CIRCUIT DIAGRAM:

**MODEL GRAPH:****TABULATION:**

Signals	Amplitude (volt)	Time period (sec)
Input signal		
Output signal		

RESULT :

Thus the Class A amplifier was constructed and observed the waveforms values are plotted in graph.

EX.NO: 8

DATE:

SIMULATION OF CE AND CS AMPLIFIER USING PSPICE

AIM:

To draw the circuit diagram of CE and CS amplifier and to simulate it using PSPICE software.

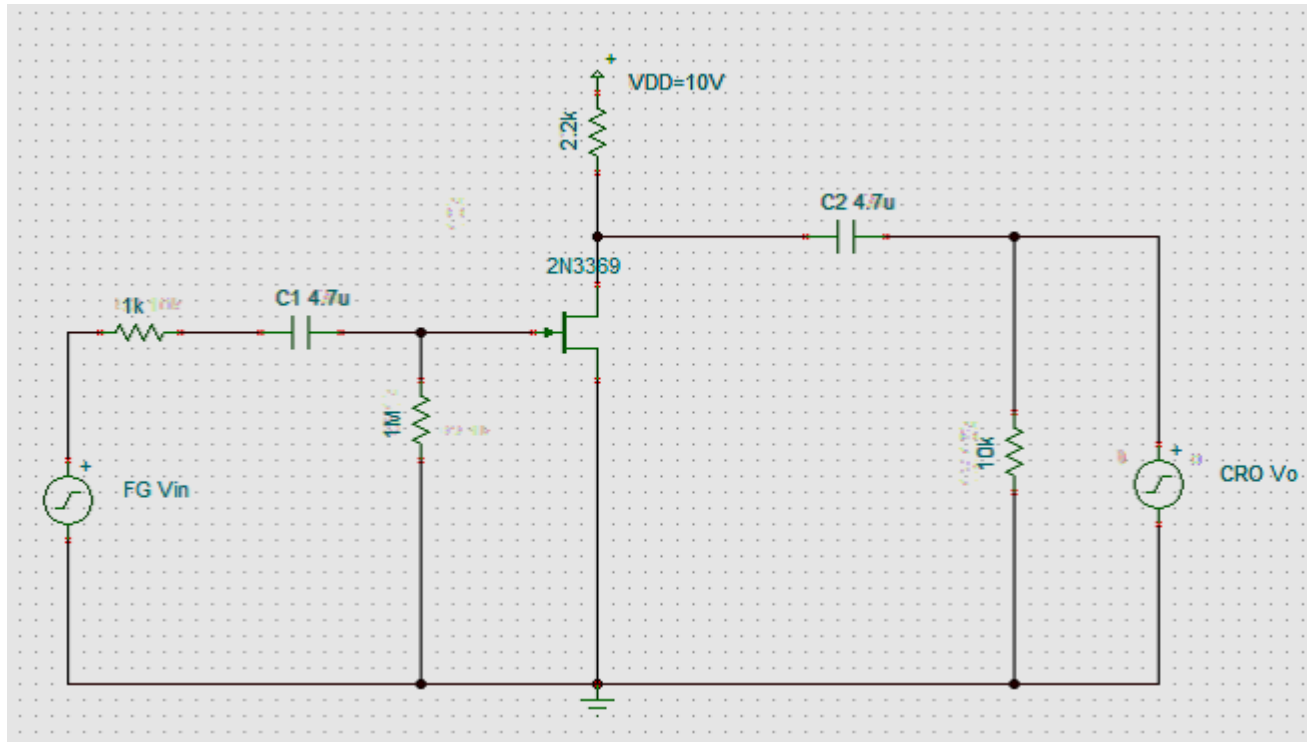
SOFTWARE TOOLS REQUIRMENTS:

1. Personal computer.
2. orcad pspice software.

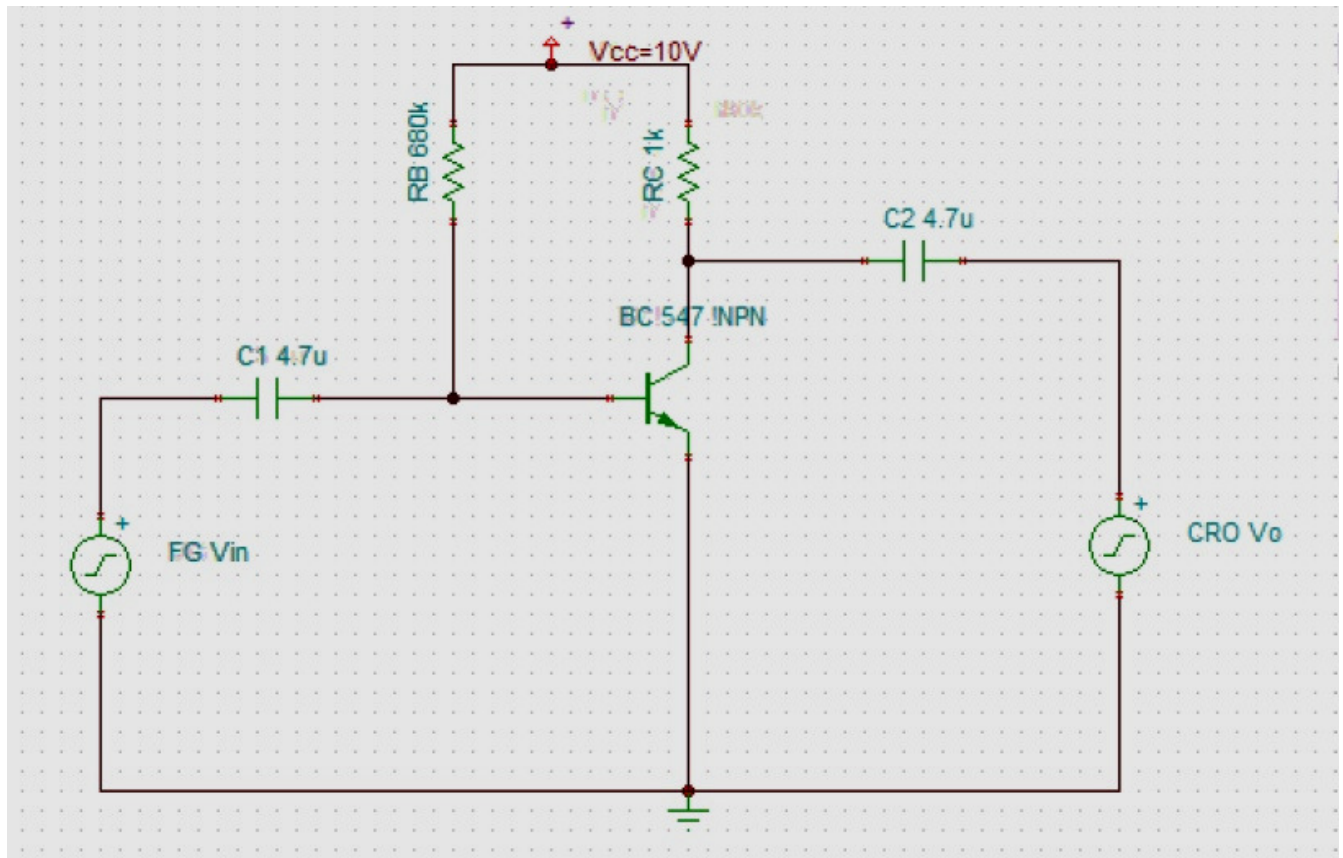
PROCEDURE:

1. Start the orcad → capture.
2. Open the new project.
3. Click and drag the components required from master database directory
4. Connect the components as per the circuit diagram.
5. Save the project.
6. Click the run symbol to simulate the circuit.
7. Click the grapher to view the output and note down the parameter.

COMMON SOURCE CIRCUIT DIAGRAM :



COMMON EMITTER CIRCUIT DIAGRAM:



RESULT:

Thus the common source and common emitter amplifier was executed and verified using Pspice.

DIGITAL EXPERIMENTS

EX. NO: 1**DATE:****STUDY OF LOGIC GATES****AIM:** -

To study about logic gates and verify their truth tables.

APPARATUS REQUIRED: -

SL No.	COMPONENT	SPECIFICATION	QTY
1.	AND GATE	IC 7408	1
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	NAND GATE 2 I/P	IC 7400	1
5.	NOR GATE	IC 7402	1
6.	X-OR GATE	IC 7486	1
7.	NAND GATE 3 I/P	IC 7410	1
8	Bread Board		1

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND and NOT are basic gates. NAND and NOR are known as universal gates. Basic gates form these gates.

AND GATE

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

X-OR GATE

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

NAND GATE

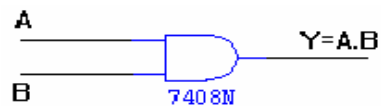
The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low. The output is low level when both inputs are high.

NOR GATE

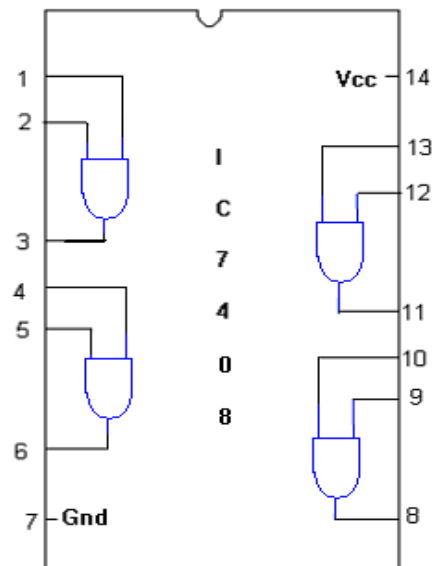
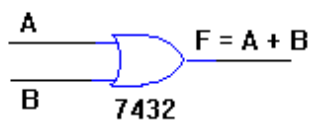
The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

PROCEDURE

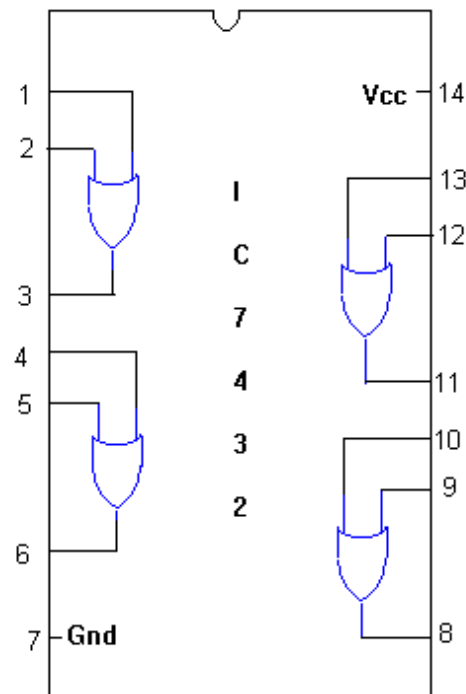
- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table.

AND GATE:**SYMBOL:****TRUTH TABLE**

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

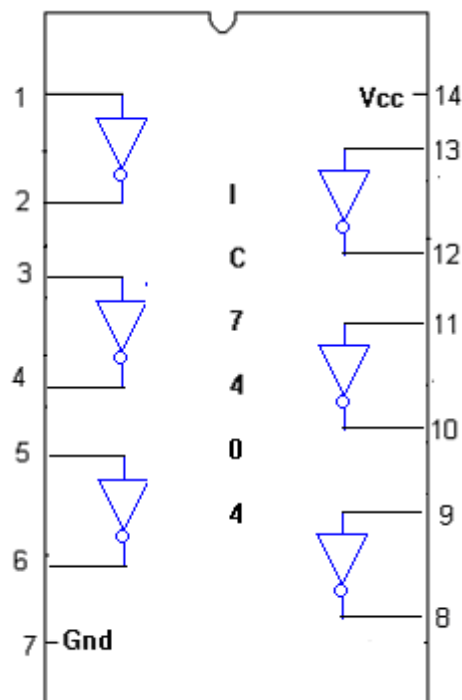
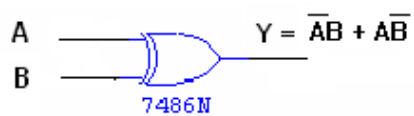
PIN DIAGRAM:**OR GATE:****SYMBOL :****TRUTH TABLE**

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

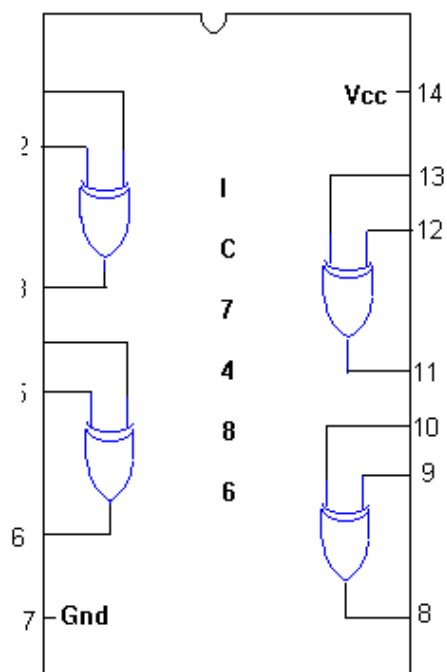
PIN DIAGRAM :

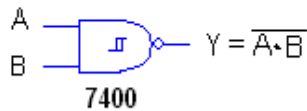
NOT GATE :**SYMBOL:****TRUTH TABLE :**

A	\overline{A}
0	1
1	0

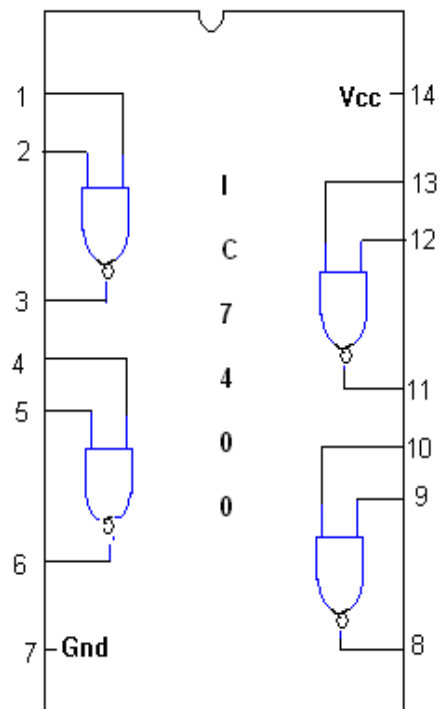
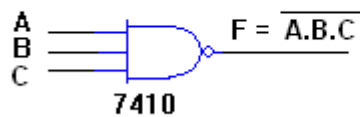
PIN DIAGRAM:**X-OR GATE :****SYMBOL :****TRUTH TABLE :**

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

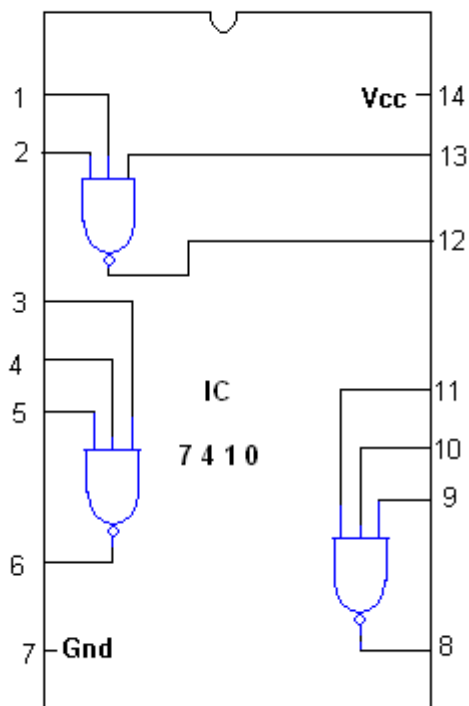
PIN DIAGRAM :

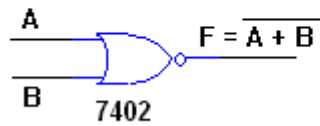
2-INPUT NAND GATE**SYMBOL****TRUTH TABLE**

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

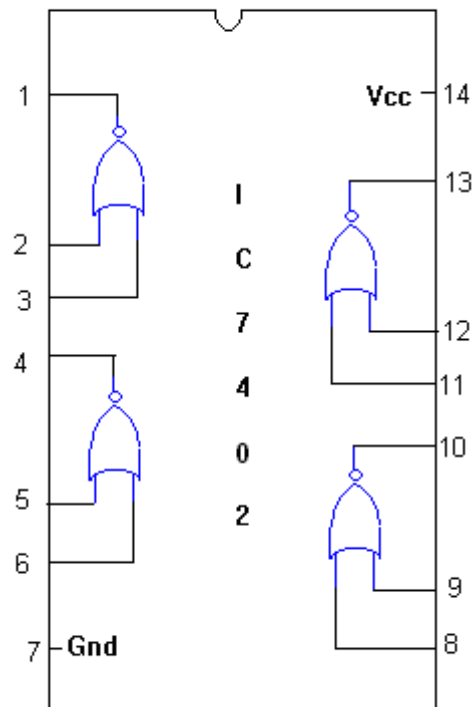
PIN DIAGRAM**3-INPUT NAND GATE****SYMBOL :****TRUTH TABLE**

A	B	C	$\overline{A \cdot B \cdot C}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

PIN DIAGRAM :

NOR GATE**SYMBOL :****TRUTH TABLE**

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

PIN DIAGRAM :**RESULT:**

Thus the logic gates were studied and their truth tables have been verified.

EX NO:2(a)**DATE:****DESIGN OF ADDER AND SUBTRACTOR****AIM:**

To design and construct half adder, full adder, half subtractor and full subtractor circuits and verify the truth table using logic gates.

APPARATUS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY
1.	AND GATE	IC 7408	1
2.	X-OR GATE	IC 7486	1
3.	NOT GATE	IC 7404	1
4.	OR GATE	IC 7432	1
5.	BREADBOARD	-	1

THEORY:**HALF ADDER:**

A half adder has two inputs for the two bits to be added and two outputs one from the sum 'S' and other from the carry 'C' into the higher adder position. Above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND gate.

FULL ADDER:

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs. A full adder is useful to add three bits at a time but a half adder cannot do so. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate

HALF SUBTRACTOR:

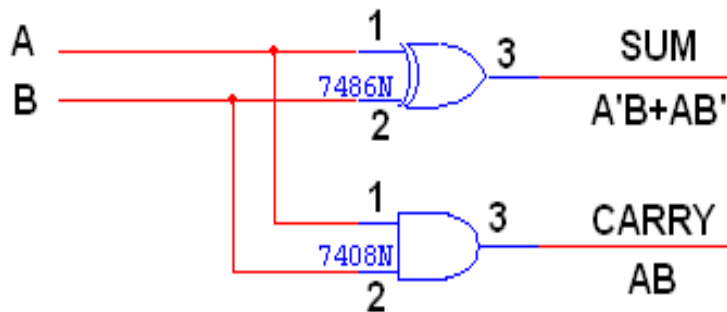
The half subtractor is constructed using X-OR and AND Gate. The half subtractor has two input and two outputs. The outputs are difference and borrow. The difference can be applied using X-OR Gate, borrow output can be implemented using an AND Gate and an inverter.

FULL SUBTRACTOR:

The full subtractor is a combination of X-OR, AND, OR, NOT Gates. In a full subtractor the logic circuit should have three inputs and two outputs. The two half subtractor put together gives a full subtractor. The first half subtractor will be C and A B. The output will be difference output of full subtractor. The expression AB assembles the borrow output of the half subtractor and the second term is the inverted difference output of first X-OR.

PROCEDURE:

- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table.

LOGIC DIAGRAM**HALF ADDER****TRUTH TABLE**

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

K-Map for SUM

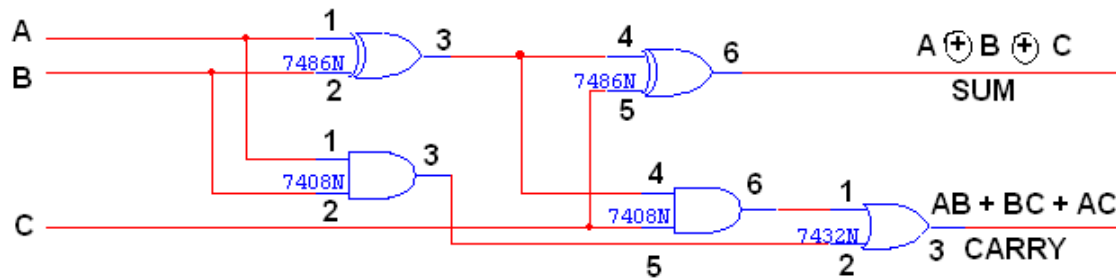
A \ B	0	1
0		1
1	1	

$$\text{SUM} = A'B + AB'$$

K-Map for CARRY

A \ B	0	1
0		
1		1

$$\text{CARRY} = AB$$

LOGIC DIAGRAM:**FULL ADDER****FULL ADDER USING TWO HALF ADDER****TRUTH TABLE:**

A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

K-Map for SUM:

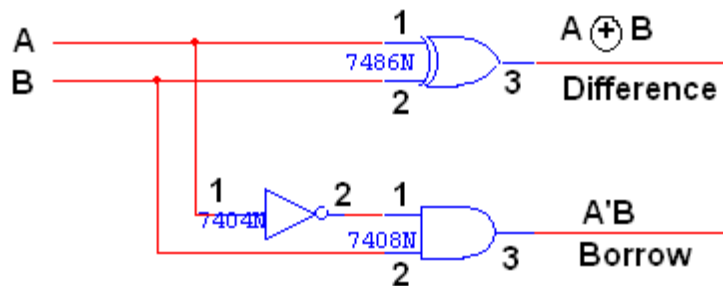
A \ BC				
	00	01	11	10
0		1		1
1	1		1	

$$\text{SUM} = A'B'C + A'BC' + ABC' + ABC$$

K-Map for CARRY:

A \ BC	BC			
	00	01	11	10
0			1	
1		1	1	1

$$\text{CARRY} = AB + BC + AC$$

LOGIC DIAGRAM:**HALF SUBTRACTOR****TRUTH TABLE:**

A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

K-Map for DIFFERENCE:

		B	
		0	1
A	0		1
	1	1	

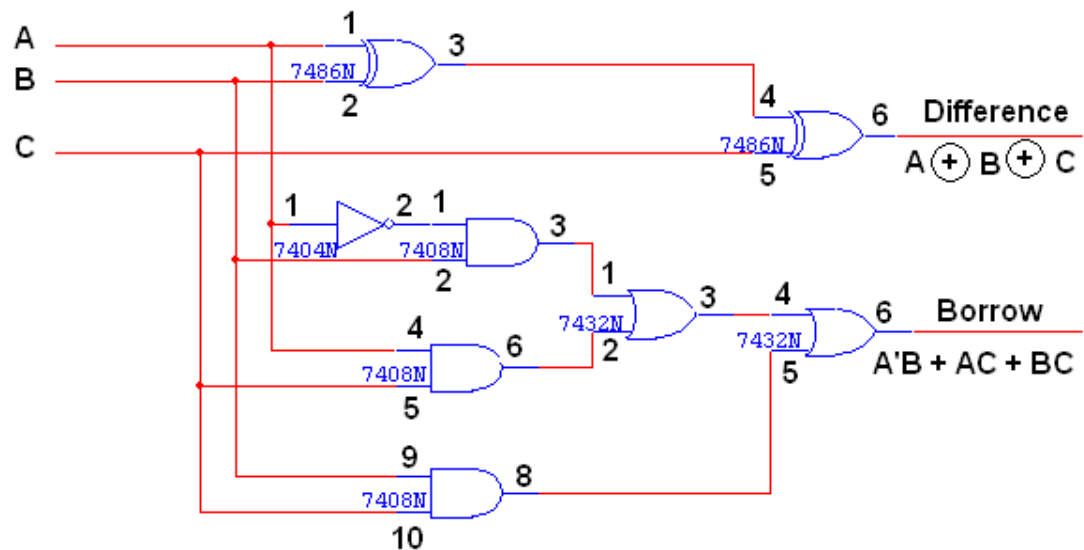
$$\text{DIFFERENCE} = A'B + AB'$$

K-Map for BORROW:

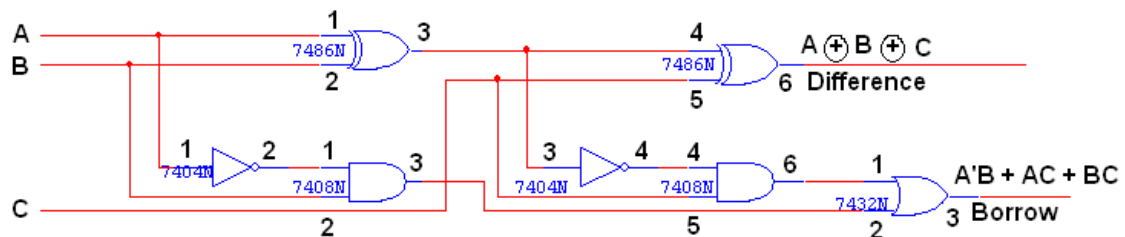
		B	
		0	1
A	0		1
	1		

$$\text{BORROW} = A'B$$

LOGIC DIAGRAM:
FULL SUBTRACTOR



FULL SUBTRACTOR USING TWO HALF SUBTRACTOR:



TRUTH TABLE:

A	B	C	BORROW	DIFFERENCE
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

--	--	--	--	--

K-Map for Difference:

A \ BC				
	00	01	11	10
0		1		1
1	1		1	

$$\text{Difference} = A'B'C + A'BC' + AB'C' + ABC$$

K-Map for Borrow:

A \ BC				
	00	01	11	10
0		1	1	1
1			1	

$$\text{Borrow} = A'B + BC + A'C$$

RESULT: -

Thus the half adder, full adder, half subtractor and full subtractor circuits were designed and their truth tables verified.

EX. NO:2(b)**DATE:****DESIGN AND IMPLEMENTATION OF CODE CONVERTORS****AIM:**

To design and implement 4-bit

- (i) Binary to gray code converter
- (ii) Gray to binary code converter
- (iii) BCD to excess-3 code converter
- (iv) Excess-3 to BCD code converter

APPARATUS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	X-OR GATE	IC 7486	1
2.	AND GATE	IC 7408	1
3.	OR GATE	IC 7432	1
4.	NOT GATE	IC 7404	1
5.	IC TRAINER KIT	-	1
6.	PATCH CORDS	-	35

THEORY:

The availability of large variety of codes for the same discrete elements of information results in the use of different codes by different systems. A conversion circuit must be inserted between the two systems if each uses different codes for same information. Thus, code converter is a circuit that makes the two systems compatible even though each uses different binary code.

The bit combination assigned to binary code to gray code. Since each code uses four bits to represent a decimal digit. There are four inputs and four outputs. Gray code is a non-weighted code.

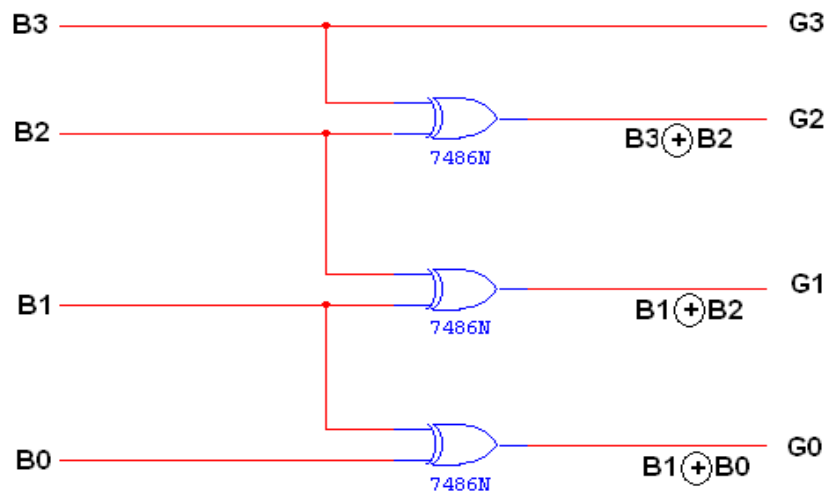
The input variables are designated as B3, B2, B1, B0 and the output variables are designated as C3, C2, C1, C0. From the truth table, a combinational circuit is designed. The Boolean functions are obtained from K-Map for each output variable.

BINARY TO EXCESS-3 CODE CONVERTOR:

A code converter is a circuit that makes the two systems compatible even though each uses a different binary code. To convert from binary code to Excess-3 code, the input lines must supply the bit combination of elements as specified by code and the output lines generate the corresponding bit combination of code. Each one of the four maps represents one of the four outputs of the circuit as a function of the four input variables.

PROCEDURE:

- (i) Connections were given as per circuit diagram.
- (ii) Logical inputs were given as per truth table
- (iii) Observe the logical output and verify with the truth tables.

LOGIC DIAGRAM:**BINARY TO GRAY CODE CONVERTOR****K-Map for G_3 :**

		B1B0			
		00	01	11	10
B3B2	00				
	01				
	11	1	1	1	1
	10	1	1	1	1

$$G_3 = B_3$$

K-Map for G_2 :

		B1B0			
		00	01	11	10
B3B2	00				
	01	1	1	1	1
	11				
	10	1	1	1	1

$G_2 = B_3 \oplus B_2$

K-Map for G_1 :

		B1B0			
		00	01	11	10
B3B2	00			1	1
	01	1	1		
	11	1	1		
	10			1	1

$G_1 = B_1 \oplus B_2$

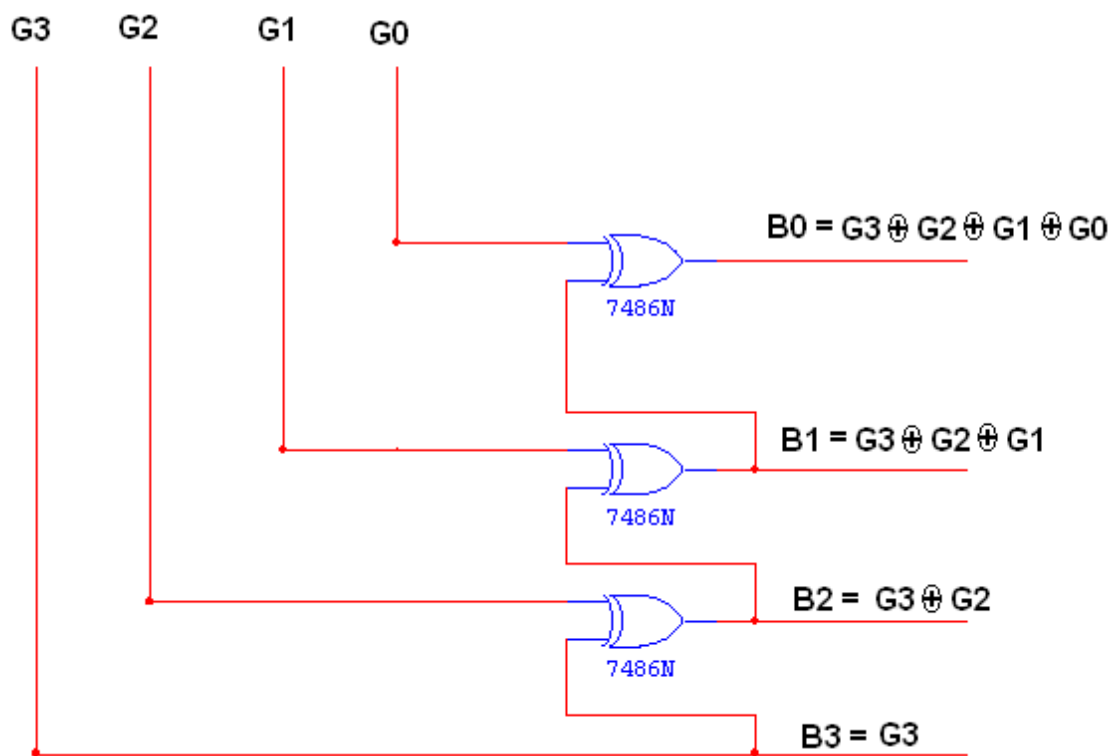
K-Map for G_0 :

B3B2 \ B1B0		00	01	11	10
00			1		1
01			1		1
11			1		1
10			1		1

$G0 = B1 \oplus B0$

TRUTH TABLE:

Binary input				Gray code output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

LOGIC DIAGRAM:**GRAY CODE TO BINARY CONVERTOR****K-Map for B_3 :**

G1G0					
G3G2		00	01	11	10
	00	0	0	0	0
	01	0	0	0	0
	11	1	1	1	1
	10	1	1	1	1

$$B_3 = G_3$$

K-Map for B_2 :

G1G0					
G3G2		00	01	11	10
	00	0	0	0	0
	01	1	1	1	1
	11	0	0	0	0
	10	1	1	1	1

$$B_2 = G_3 \oplus G_2$$

K-Map for B_1 :

G3G2 \ G1G0		G1G0			
		00	01	11	10
G3G2	00	0	0	1	1
	01	1	1	0	0
	11	0	0	1	1
	10	1	1	0	0

$$B1 = G3 \oplus G2 \oplus G1$$

K-Map for B_0 :

G3G2 \ G1G0		G1G0			
		00	01	11	10
G3G2	00	0	①	0	①
	01	①	0	①	0
	11	0	①	0	①
	10	①	0	①	0

$$B0 = G3 \oplus G2 \oplus G1 \oplus G0$$

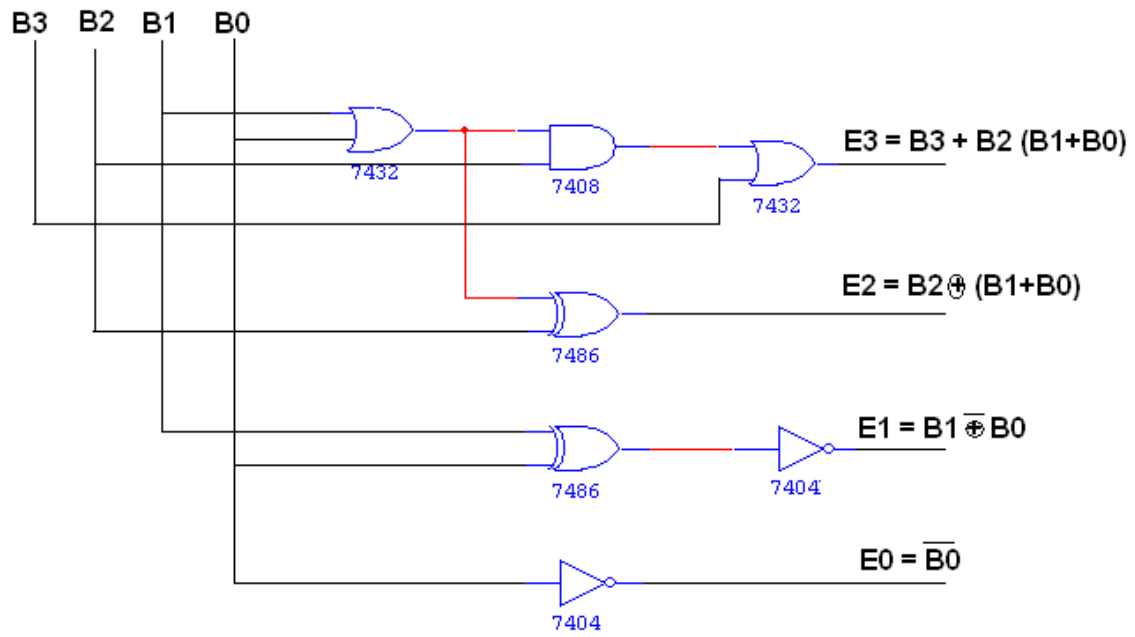
TRUTH TABLE:

Gray Code				Binary Code			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0

0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

LOGIC DIAGRAM:

BCD TO EXCESS-3 CONVERTOR



K-Map for E₃:

		B1B0			
		00	01	11	10
B3B2	00				
	01		1	1	1
	11	x	x	x	x
	10	1	1	x	x

$$E3 = B3 + B2 (B0 + B1)$$

K-Map for E_2 :

		B1B0			
		00	01	11	10
B3B2	00		1	1	1
	01	1			
	11	x	x	x	x
	10		1	x	x

$$E_2 = B_2 \oplus (B_1 + B_0)$$

K-Map for E_1 :

		B1B0			
		00	01	11	10
B3B2	00	1		1	
	01	1		1	
	11	x	x	x	x
	10	1		x	x

$$E_1 = B_1 \oplus B_0$$

K-Map for E_0 :

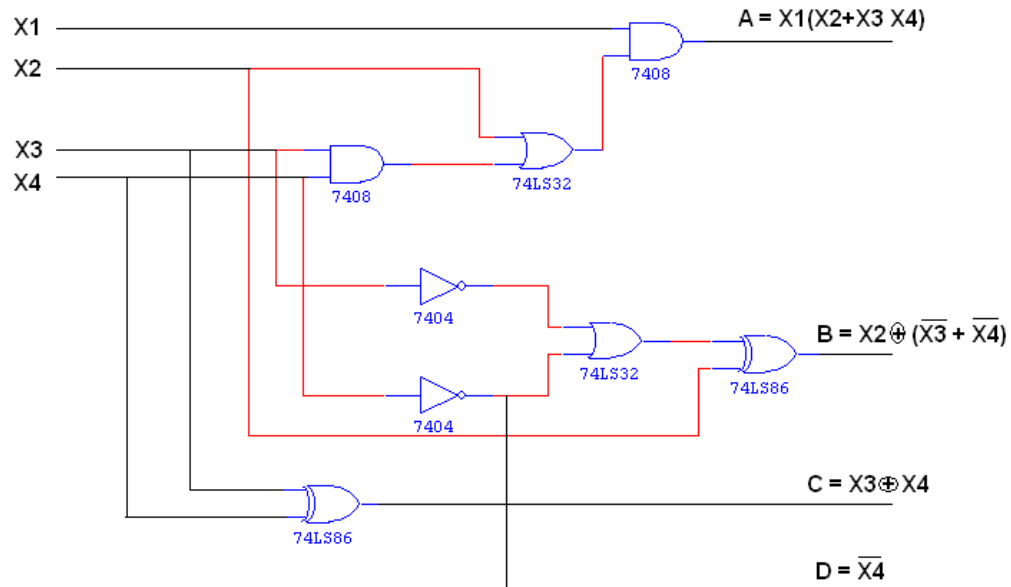
B3B2 \ B1B0		B1B0			
		00	01	11	10
B3B2	00	1			1
	01	1			1
	11	x	x	x	x
	10	1		x	x

$$E0 = \overline{B0}$$

TRUTH TABLE:

BCD input				Excess – 3 output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

LOGIC DIAGRAM:**EXCESS-3 TO BCD CONVERTOR**



K-Map for A:

X1 X2 \ X3 X4					
		00	01	11	10
X1 X2	00	X	X	0	X
	01	0	0	0	0
	11	1	X	X	X
	10	0	0	1	0

$$A = X1 X2 + X3 X4 X1$$

K-Map for B:

X3 X4 X1 X2		00	01	11	10
		00	01	11	10
00	X	X	0	X	
01	0	0	1	0	
11	0	X	X	X	
10	1	1	0	1	

$$B = X2 \oplus (\overline{X3} + \overline{X4})$$

K-Map for C:

X1 X2 \ X3 X4					
		00	01	11	10
X1 X2	00	X	X	0	X
	01	0	1	X	1
	11	0	X	X	X
	10	X	1	0	1

$$C = X3 \oplus X4$$

K-Map for D:

X1 X2 \ X3 X4					
		00	01	11	10
X1 X2	00	X	X	0	X
	01	1	0	0	1
	11	1	X	X	X
	10	1	0	0	1

$$D = \overline{X_4}$$

TRUTH TABLE:

Excess – 3 Input				BCD Output			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

RESULT: -

Thus the code converter circuits were designed and their logic verified.

EX NO:3

DATE:**DESIGN OF 4-BIT ADDER AND SUBTRACTOR****AIM:**

To design and implement the 4-bit adder and subtractor using IC 7483.

APPARATUS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	IC	IC 7483	1
2.	EX-OR GATE	IC 7486	1
3.	NOT GATE	IC 7404	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	40

THEORY:**4 BIT BINARY ADDER:**

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of next full adder in chain. The augends bits of 'A' and the addend bits of 'B' are designated by subscript numbers from right to left, with subscript 0 denoting the least significant bits. The carries are connected in chain through the full adder. The input carry to the adder is C_0 and it ripples through the full adder to the output carry C_4 .

4 BIT BINARY SUBTRACTOR:

The circuit for subtracting $A-B$ consists of an adder with inverters, placed between each data input 'B' and the corresponding input of full adder. The input carry C_0 must be equal to 1 when performing subtraction.

4 BIT BINARY ADDER/SUBTRACTOR:

The addition and subtraction operation can be combined into one circuit with one common binary adder. The mode input M controls the operation. When $M=0$, the circuit is adder circuit. When $M=1$, it becomes subtractor.

4 BIT BCD ADDER:

Consider the arithmetic addition of two decimal digits in BCD, together with an input carry from a previous stage. Since each input digit does not exceed 9, the output sum cannot be greater than 19, the 1 in the sum being an input carry. The output of two decimal digits must be represented in BCD and should appear in the form listed in the columns.

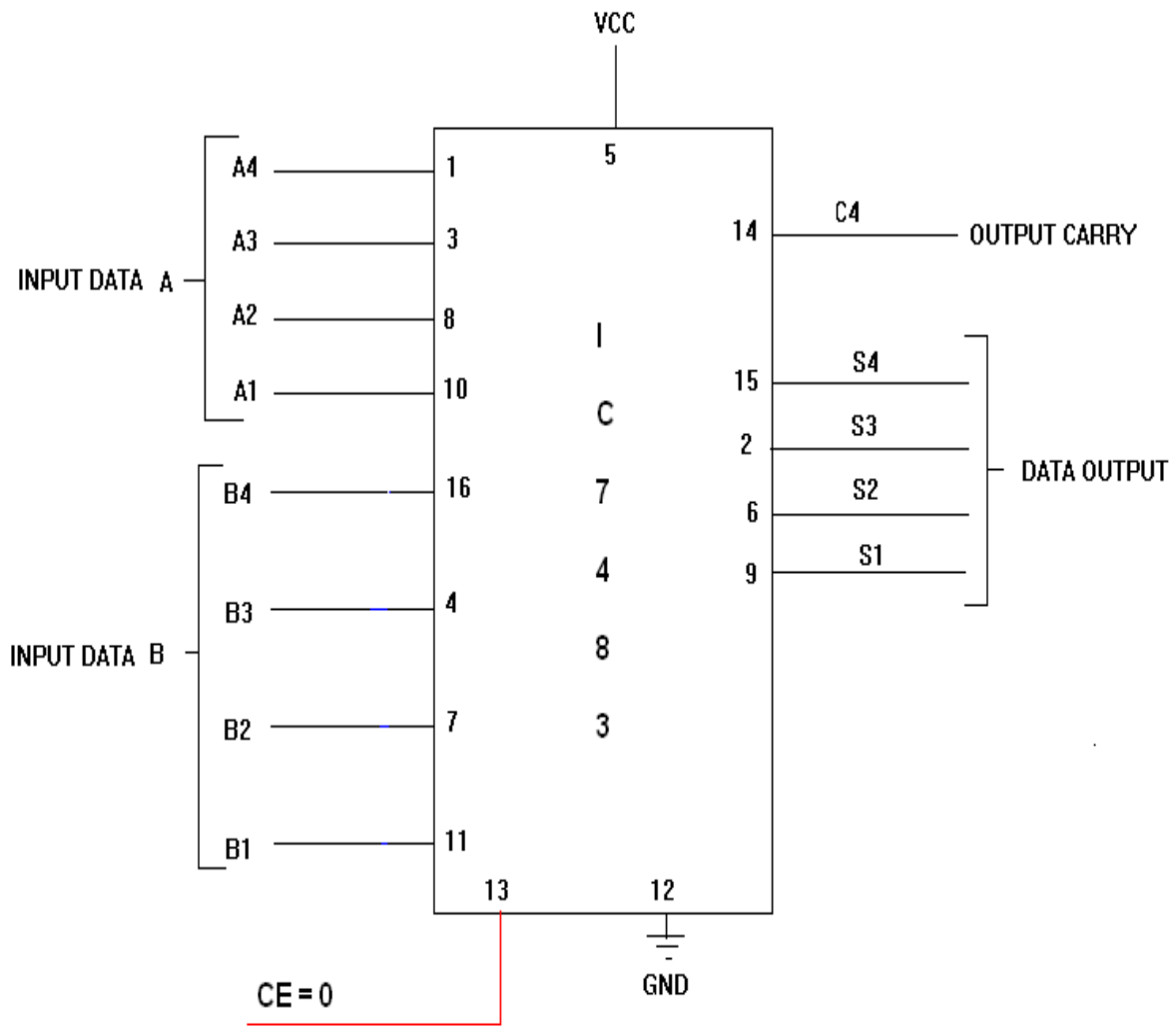
ABCD adder that adds 2 BCD digits and produce a sum digit in BCD. The 2 decimal digits, together with the input carry, are first added in the top 4 bit adder to produce the binary sum.

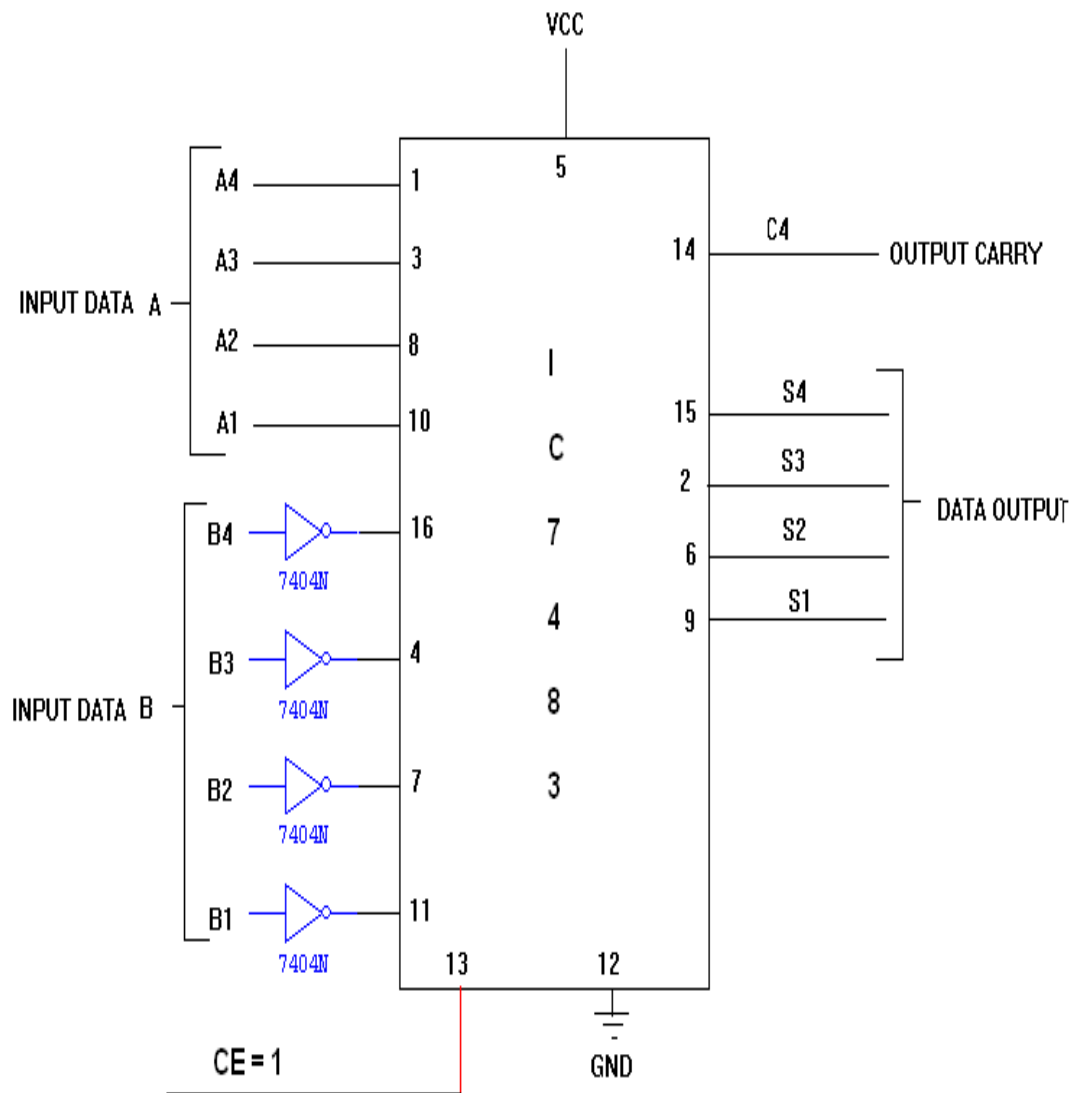
PROCEDURE:

Connections were given as per circuit diagram.

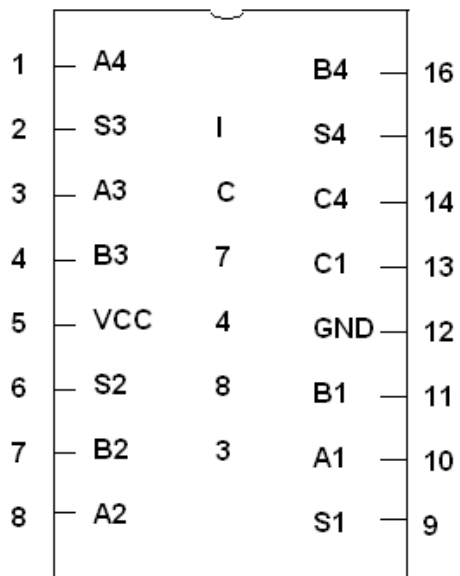
- (i) Logical inputs were given as per truth table
- (ii) Observe the logical output and verify with the truth tables.
- (iii) **LOGIC DIAGRAM:**

4-BIT BINARY ADDER

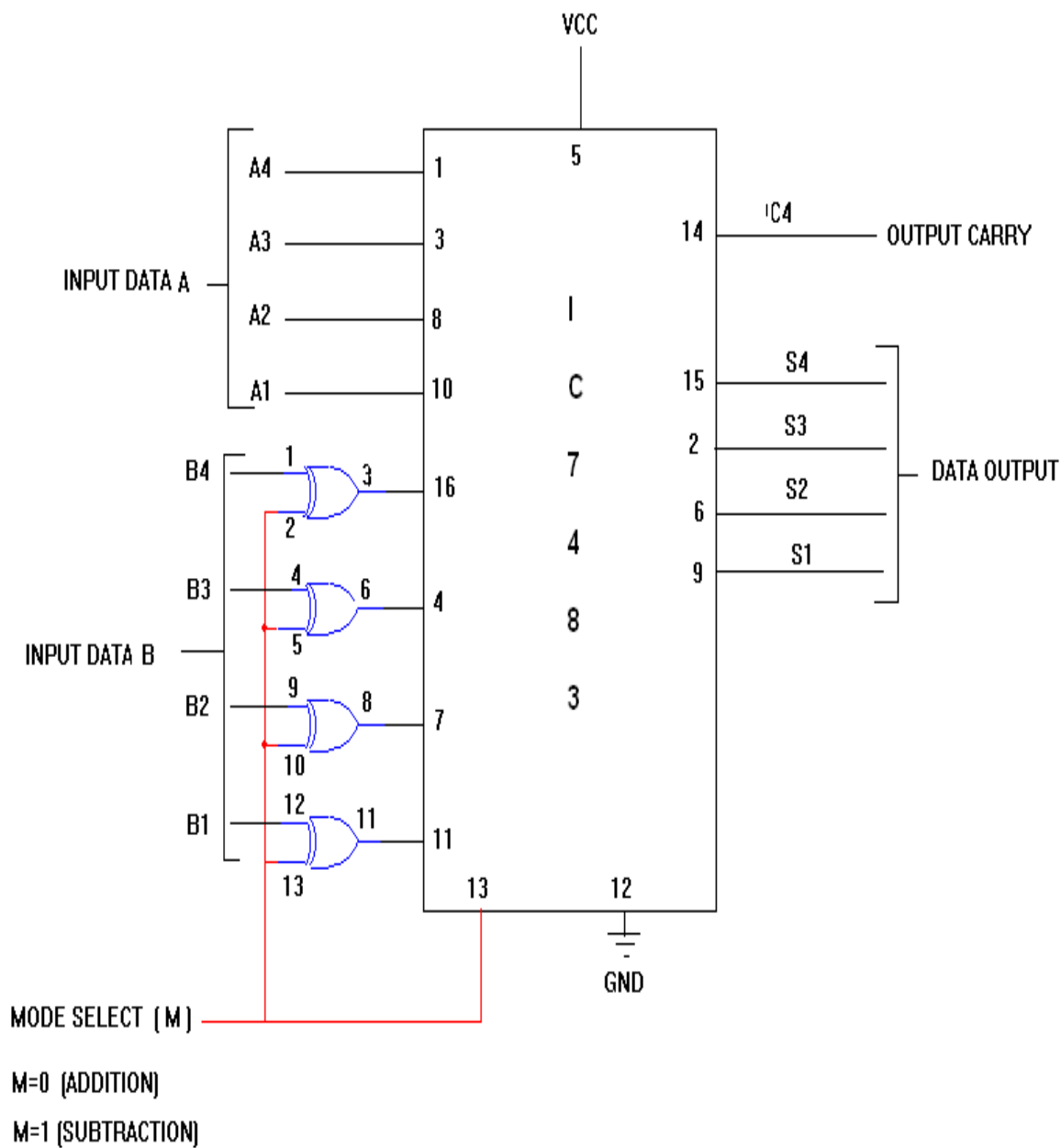


LOGIC DIAGRAM:**4-BIT BINARY SUBTRACTOR**

PIN DIAGRAM FOR IC 7483:



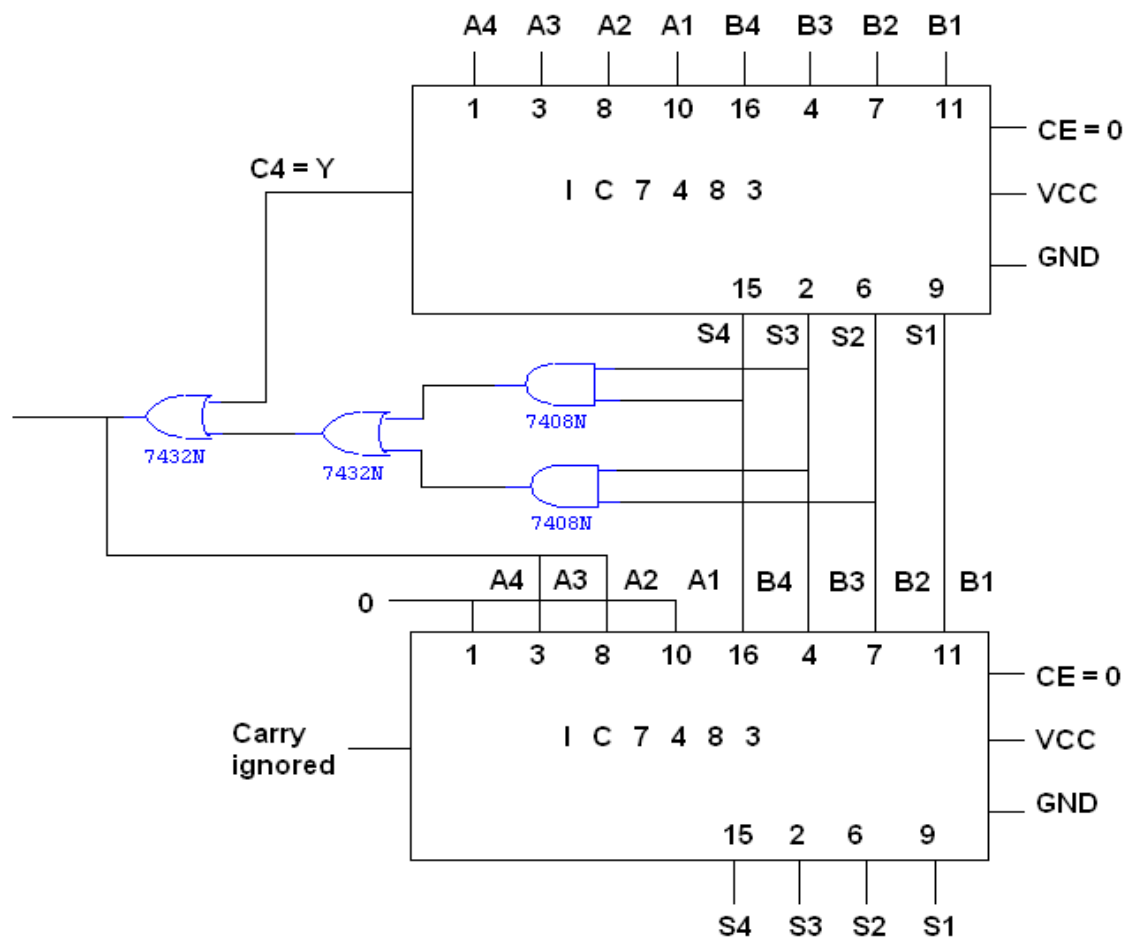
LOGIC DIAGRAM:
4-BIT BINARY ADDER/SUBTRACTOR



TRUTH TABLE:

Input Data A				Input Data B				Addition					Subtraction				
A4	A3	A2	A1	B4	B3	B2	B1	C	S4	S3	S2	S1	B	D4	D3	D2	D1
1	0	0	0	0	0	1	0	0	1	0	1	0	1	0	1	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	0	1	0	0	1	1	1	1
1	1	1	0	1	1	1	1	1	1	0	1	0	0	1	1	1	1
1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	1	0	1

LOGIC DIAGRAM:
BCD ADDER



K MAP

S3 S4		S1 S2			
		00	01	11	10
00	0	0	0	0	0
01	0	0	0	0	0
11	1	1	1	1	
10	0	0	1	1	

$$Y = S4 (S3 + S2)$$

TRUTH TABLE:

BCD SUM				CARRY
S4	S3	S2	S1	C
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

RESULT: -

Thus the 4 bit adder and subtractor circuits were designed and their logic was verified.

EX NO: 4**DATE:****DESIGN AND IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER****AIM:**

To design and implement multiplexer and demultiplexer using logic gates and study of IC 74150 and IC 74154.

APPARATUS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	3 I/P AND GATE	IC 7411	2
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	32

THEORY:**MULTIPLEXER:**

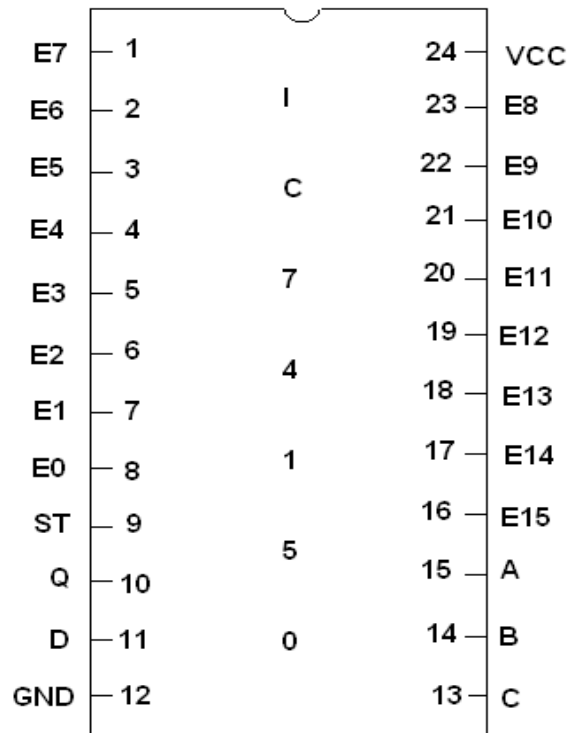
Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input line and n selection lines whose bit combination determine which input is selected.

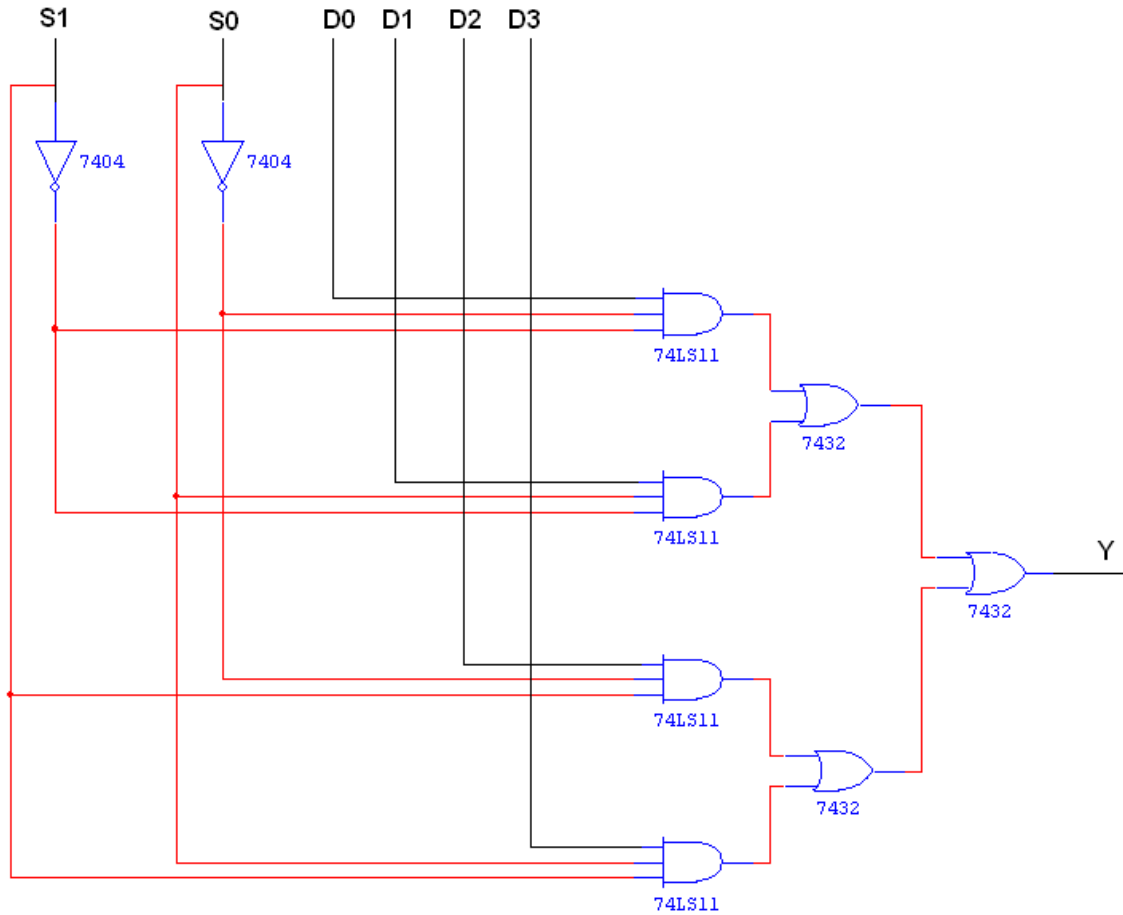
The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as Demultiplexer.

In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

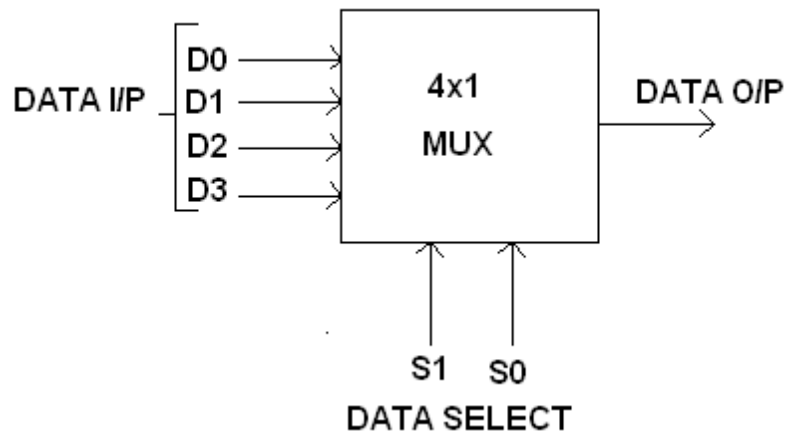
PROCEDURE:

- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table.

PIN DIAGRAM FOR IC 74150:

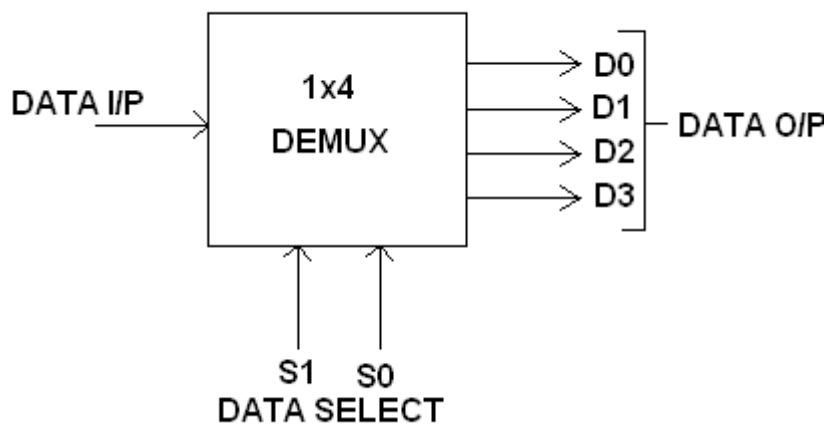
CIRCUIT DIAGRAM FOR 4X1 MULTIPLEXER:**TRUTH TABLE:**

S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:**FUNCTION TABLE:**

S1	S0	INPUTS Y
0	0	$D0 \rightarrow D0 S1' S0'$
0	1	$D1 \rightarrow D1 S1' S0$
1	0	$D2 \rightarrow D2 S1 S0'$
1	1	$D3 \rightarrow D3 S1 S0$

$$Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0$$

BLOCK DIAGRAM FOR 1:4 DEMULTIPLEXER:**FUNCTION TABLE:**

S1	S0	INPUT
0	0	$X \rightarrow D0 = X S1' S0'$
0	1	$X \rightarrow D1 = X S1' S0$
1	0	$X \rightarrow D2 = X S1 S0'$
1	1	$X \rightarrow D3 = X S1 S0$

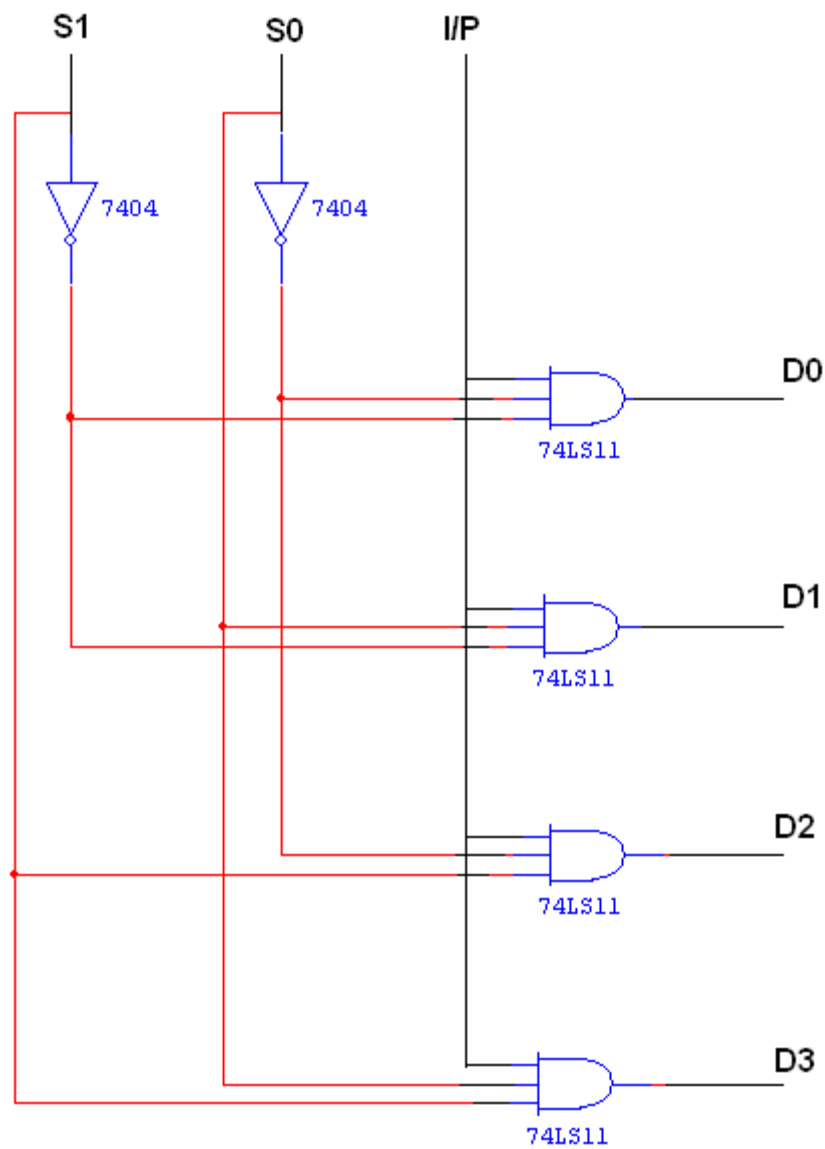
$$D0 = X S1' S0'$$

$$D1 = X S1' S0$$

$$D2 = X S1 S0'$$

$$D3 = X S1 S0$$

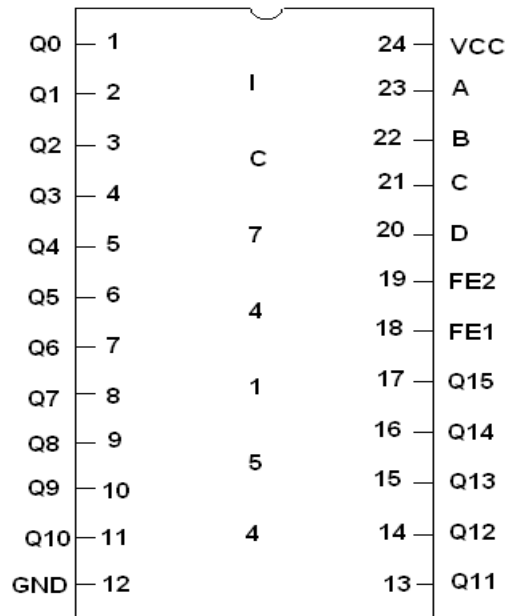
LOGIC DIAGRAM FOR DEMULTIPLEXER:



TRUTH TABLE:

INPUT			OUTPUT			
S1	S0	I/P	D0	D1	D2	D3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

.

PIN DIAGRAM FOR IC 74154:**RESULT: -**

Thus the Multiplexer/Demultiplexer circuits were designed and their logic was verified.

EX NO:5**DATE:****DESIGN AND IMPLEMENTATION OF ENCODER AND DECODER****AIM:**

To design and implement encoder and decoder using logic gates , study of IC 7445 and IC 74147.

APPARATUS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	3 I/P NAND GATE	IC 7410	2
2.	OR GATE	IC 7432	3
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	27

THEORY:**ENCODER:**

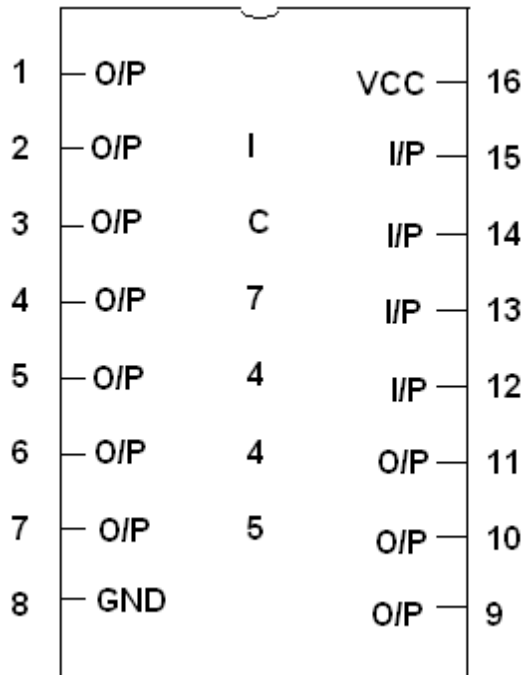
An encoder is a digital circuit that performs inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generates the binary code corresponding to the input value. In octal to binary encoder it has eight inputs, one for each octal digit and three output that generate the corresponding binary code. In encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguity that when all inputs are zero the outputs are zero. The zero outputs can also be generated when $D_0 = 1$.

DECODER:

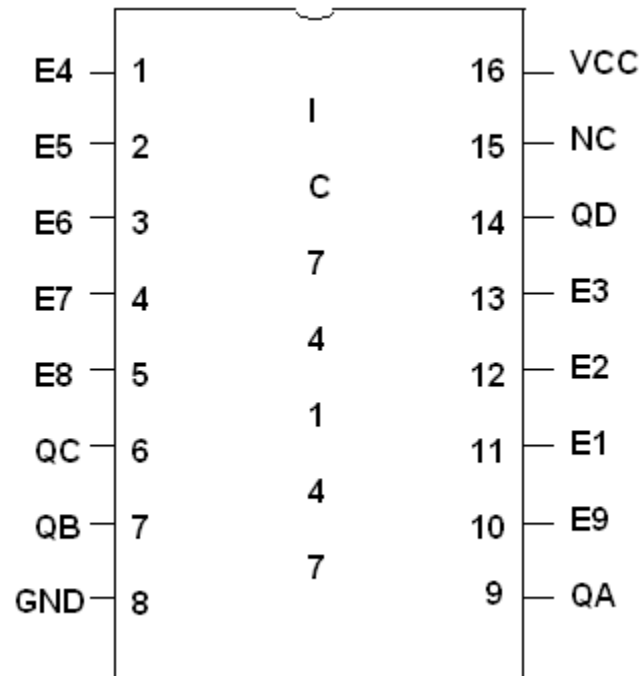
A decoder is a multiple input multiple output logic circuit which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e there is one to one mapping can be expressed in truth table. In the block diagram of decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through out $2^n - 1$.

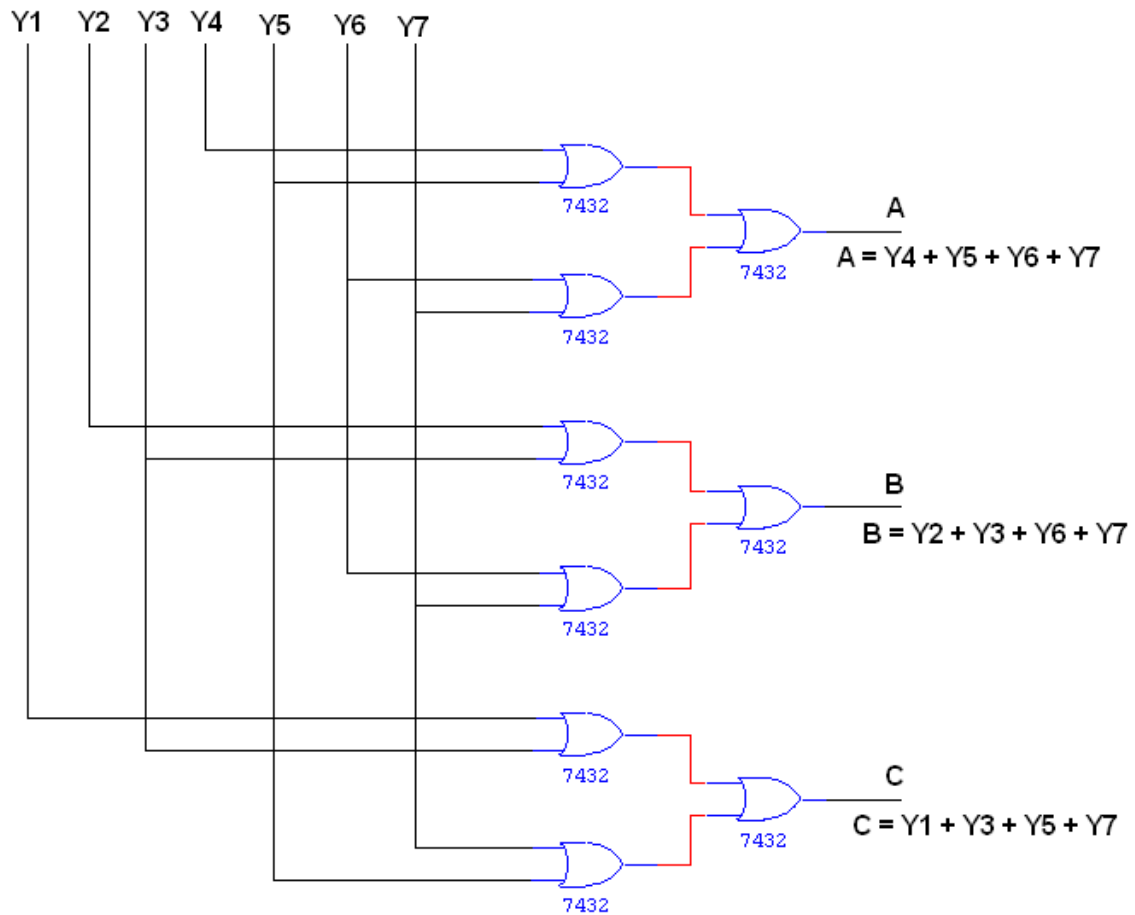
PROCEDURE:

- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table
- (iv)

PIN DIAGRAM FOR IC 7445:**BCD TO DECIMAL DECODER:**

PIN DIAGRAM FOR IC 74147:

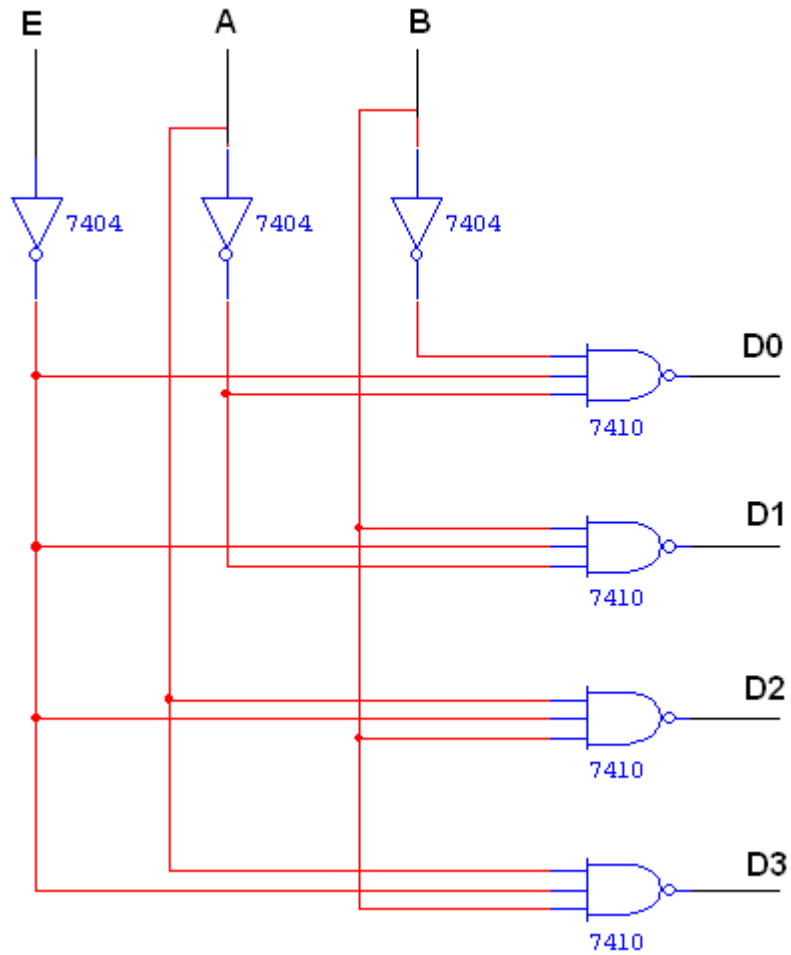


LOGIC DIAGRAM FOR ENCODER:

TRUTH TABLE:

INPUT							OUTPUT		
Y1	Y2	Y3	Y4	Y5	Y6	Y7	A	B	C
1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	1	1	1	1

LOGIC DIAGRAM FOR DECODER:



TRUTH TABLE:

INPUT			OUTPUT			
E	A	B	D0	D1	D2	D3
1	0	0	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

RESULT: -

Thus the encoder/decoder circuits were designed and their logic was verified

EX NO:6**DATE:****CONSTRUCTION AND VERIFICATION OF 4 BIT RIPPLE COUNTER AND MOD 10/MOD 12 RIPPLE COUNTER****AIM:**

To design and verify 4 bit ripple counter and Mod 10/ Mod 12 ripple counter.

APPARATUS REQUIRED:

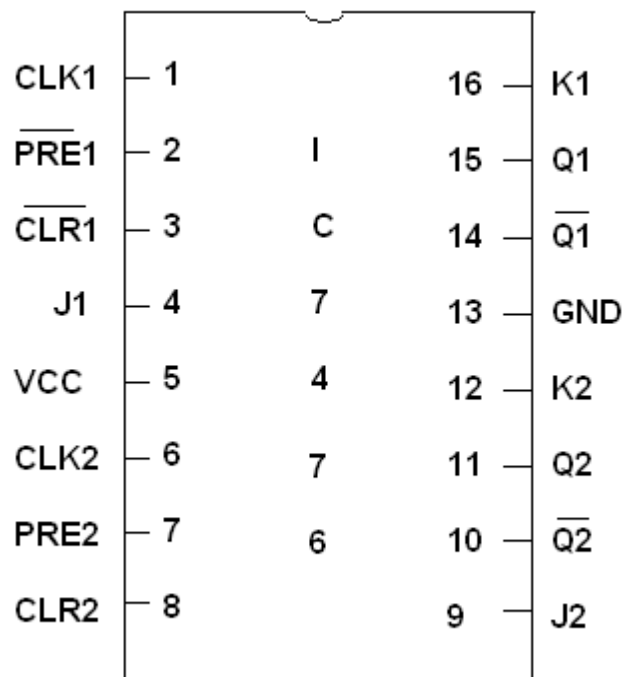
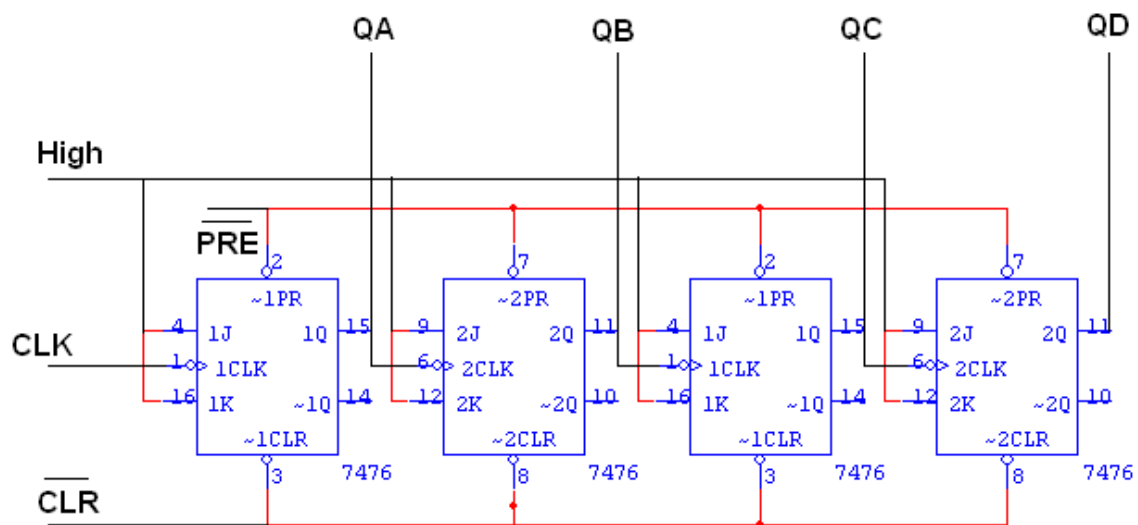
Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	JK FLIP FLOP	IC 7476	2
2.	NAND GATE	IC 7400	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	30

THEORY:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between a register and a counter. There are two types of counter, synchronous and asynchronous. In synchronous common clock is given to all flip flop and in asynchronous first flip flop is clocked by external pulse and then each successive flip flop is clocked by Q or \bar{Q} output of previous stage. As soon the clock of second stage is triggered by output of first stage. Because of inherent propagation delay time all flip flops are not activated at same time which results in asynchronous operation.

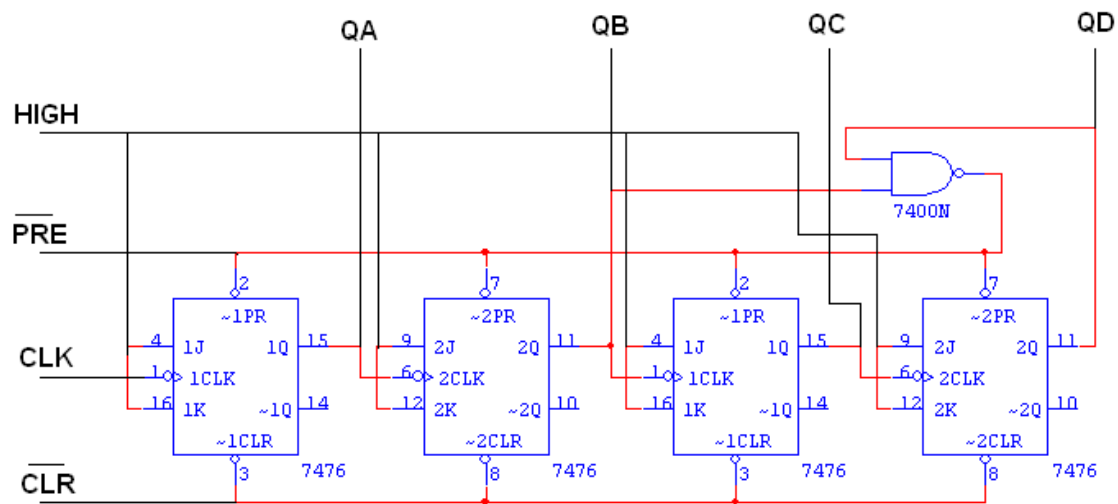
PROCEDURE:

- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table.

PIN DIAGRAM FOR IC 7476:**LOGIC DIAGRAM FOR 4 BIT RIPPLE COUNTER:**

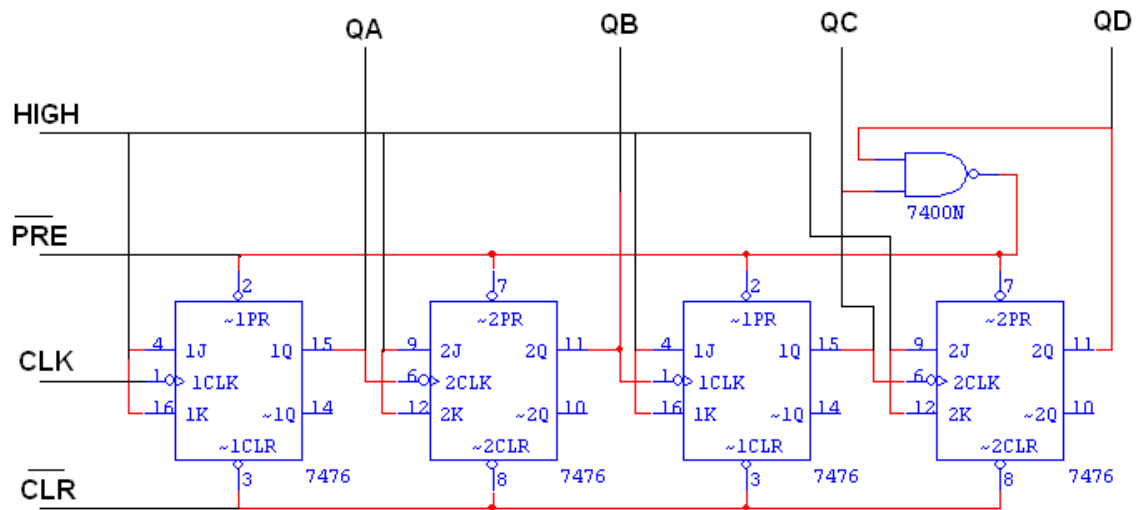
TRUTH TABLE:

CLK	QD	QC	QB	QA
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

LOGIC DIAGRAM FOR MOD - 10 RIPPLE COUNTER:

TRUTH TABLE:

CLK	QD	QC	QB	QA
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0

LOGIC DIAGRAM FOR MOD - 12 RIPPLE COUNTER:

TRUTH TABLE:

CLK	QD	QC	QB	QA
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	0	0

RESULT: -

Thus the 4bit ripple counter and Mod counter circuits were designed and their logic was verified.

EX NO:7**DATE:****DESIGN AND IMPLEMENTATION OF 3 BIT SYNCHRONOUS UP/DOWN COUNTER****AIM:**

To design and implement the 3 bit synchronous up/down counter.

APPARATUS REQUIRED:

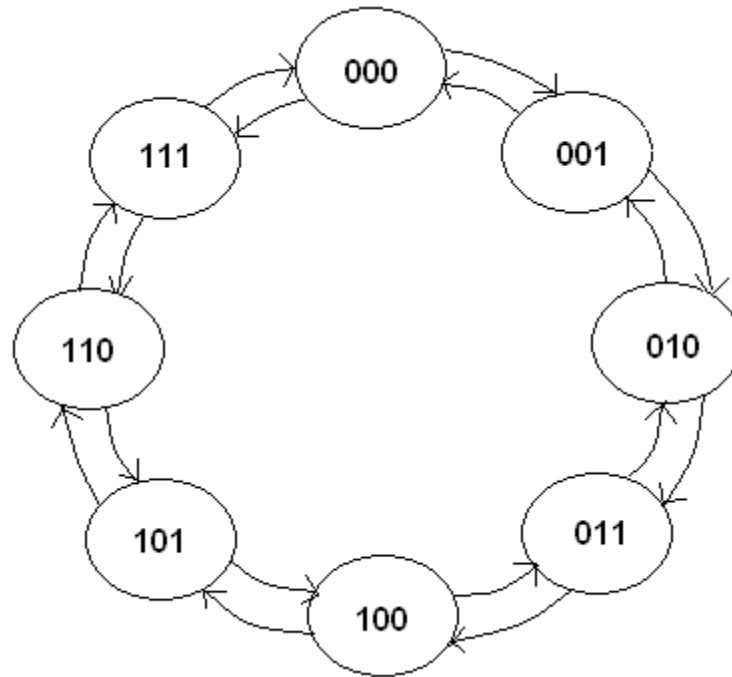
Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	JK FLIP FLOP	IC 7476	2
2.	3 I/P AND GATE	IC 7411	1
3.	OR GATE	IC 7432	1
4.	XOR GATE	IC 7486	1
5.	NOT GATE	IC 7404	1
6.	IC TRAINER KIT	-	1
7.	PATCH CORDS	-	35

THEORY:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

PROCEDURE:

- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table

STATE DIAGRAM:**CHARACTERISTICS TABLE:**

Q	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

TRUTH TABLE:

Input Up/Down	Present State			Next State			A		B		C	
	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	1	1	1	X	1	X	1	X
0	1	1	1	1	1	0	X	0	X	0	X	1
0	1	1	0	1	0	1	X	0	X	1	1	X
0	1	0	1	1	0	0	X	0	0	X	X	1
0	1	0	0	0	1	1	X	1	1	X	1	X
0	0	1	1	0	1	0	0	X	X	0	X	1
0	0	1	0	0	0	1	0	X	X	1	1	X
0	0	0	1	0	0	0	0	X	0	X	X	1
1	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
1	0	1	0	0	1	1	0	X	X	0	1	X
1	0	1	1	1	0	0	1	X	X	1	X	1
1	1	0	0	1	0	1	X	0	0	X	1	X
1	1	0	1	1	1	0	X	0	1	X	X	1
1	1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	0	0	X	1	X	1	X	1

K MAP

		QB QC			
		00	01	11	10
UD QA	00	1	0	0	0
	01	X	X	X	X
	11	X	X	X	X
	10	0	0	1	0

$$JA = \overline{UD} \overline{QB} \overline{QC} + UD QB QC$$

		QB QC			
		00	01	11	10
UD QA	00	X	X	X	X
	01	1	0	0	0
	11	0	0	1	0
	10	X	X	X	X

$$KA = \overline{UD} \overline{QB} \overline{QC} + UD QB QC$$

		QB QC			
		00	01	11	10
UD QA	00	1	X	X	1
	01	1	X	X	1
	11	1	X	X	1
	10	1	X	X	1

$$JC = 1$$

K MAP

		QB QC			
		00	01	11	10
UD QA	00	1	0	X	X
	01	1	0	X	X
	11	0	1	X	X
	10	0	1	X	X

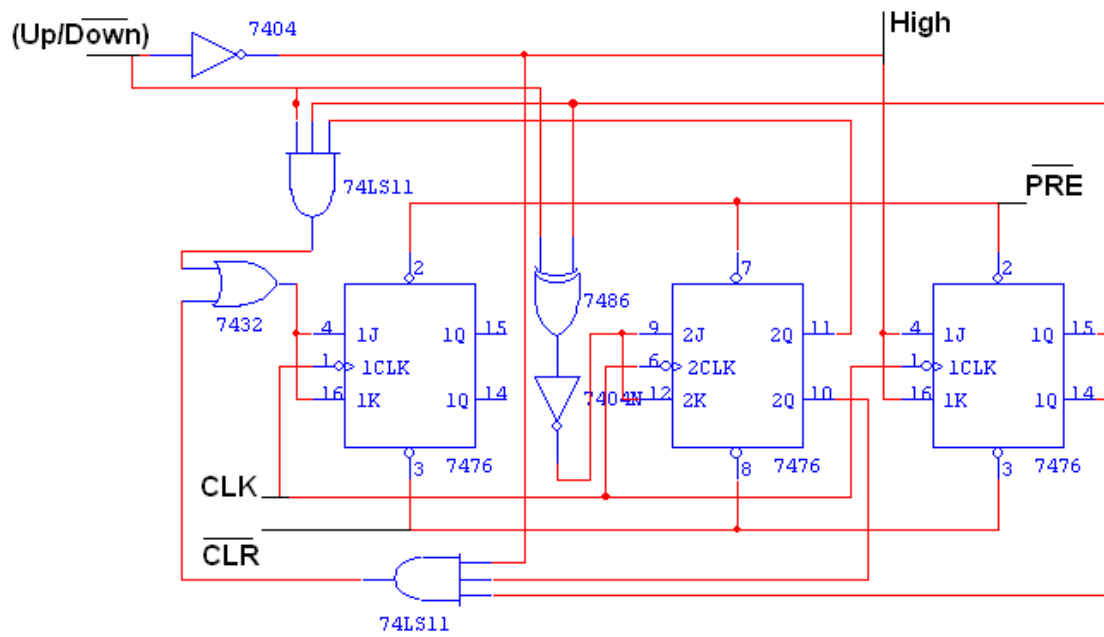
$$JB = \overline{UD} \oplus QC$$

		QB QC			
		00	01	11	10
UD QA	00	X	X	0	1
	01	X	X	0	1
	11	X	X	1	0
	10	X	X	1	0

$$KB = \overline{UD} \oplus QC$$

		QB QC			
		00	01	11	10
UD QA	00	X	1	1	X
	01	X	1	1	X
	11	X	1	1	X
	10	X	1	1	X

$$KC = 1$$

LOGIC DIAGRAM:**RESULT: -**

Thus the 3 bit synchronous up/down counter circuits were designed and their logic was verified.

EX. NO:8**DATE:****DESIGN AND IMPLEMENTATION OF SHIFT REGISTER****AIM:**

To design and implement

- (i) Serial in serial out
- (ii) Serial in parallel out
- (iii) Parallel in serial out
- (iv) Parallel in parallel out

APPARATUS REQUIRED:

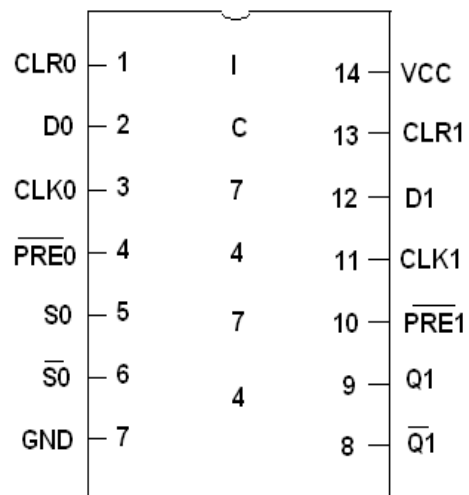
Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	D FLIP FLOP	IC 7474	2
2.	OR GATE	IC 7432	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	35

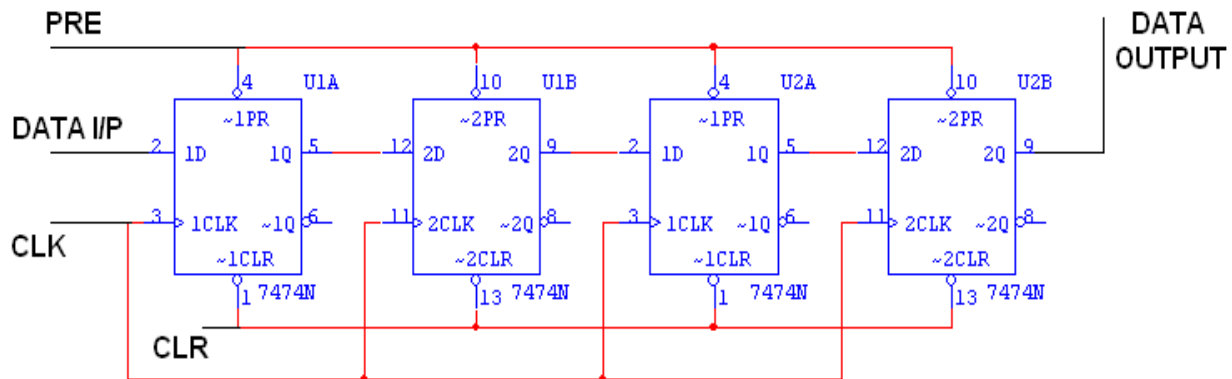
THEORY:

A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop. The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to right.

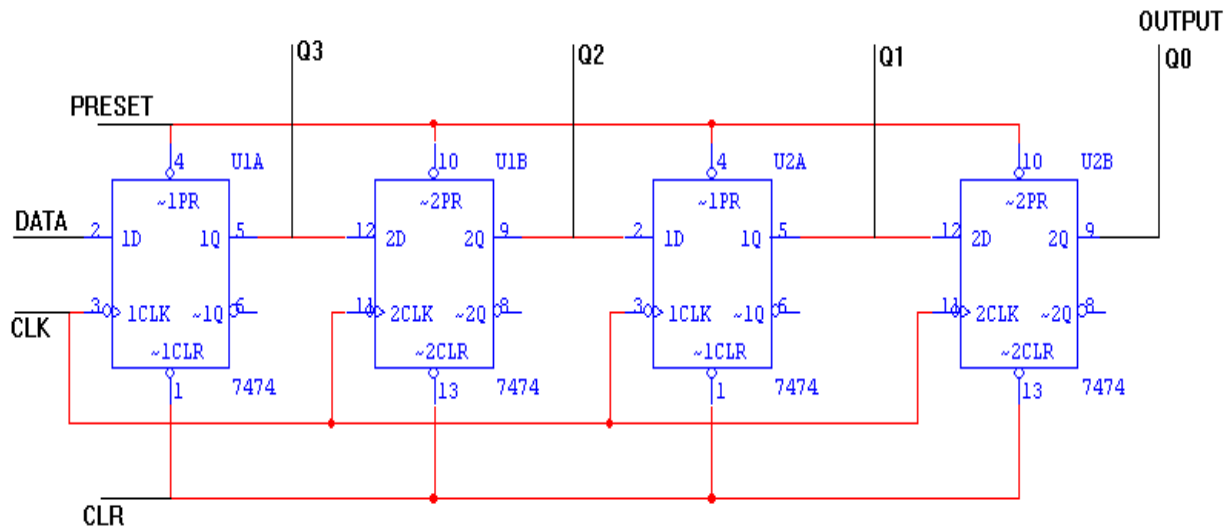
PROCEDURE:

- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table.

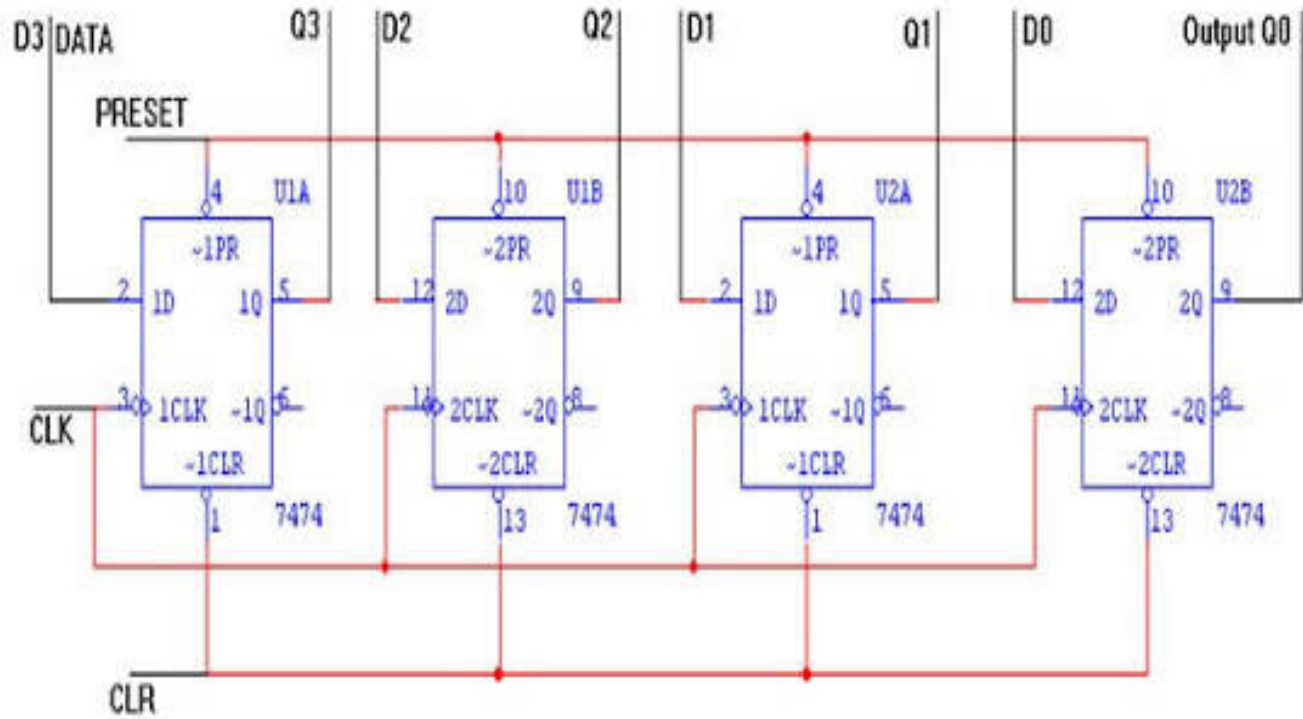
PIN DIAGRAM:

LOGIC DIAGRAM:**SERIAL IN SERIAL OUT:****TRUTH TABLE:**

CLK	Serial in	Serial out
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

LOGIC DIAGRAM:**SERIAL IN PARALLEL OUT:****TRUTH TABLE (SERIAL IN PARALLEL OUT):**

CLK	DATA	OUTPUT			
		Q _A	Q _B	Q _C	Q _D
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0
4	1	1	0	0	1

LOGIC DIAGRAM:**PARALLEL IN PARALLEL OUT:****TRUTH TABLE:**

CLK	DATA INPUT				OUTPUT			
	D _A	D _B	D _C	D _D	Q _A	Q _B	Q _C	Q _D
1	1	0	0	1	1	0	0	1
2	0	1	0	1	0	1	0	1
3	0	0	0	1	0	0	0	1
4	1	1	1	1	1	1	1	1
5	0	0	0	0	0	0	0	0

RESULT: -

Thus the shift register circuits were designed and their logic was verified